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12 GHZ MIXER/LOCAL OSCILLATOR AND PARAMETRIC AMPLIFIER

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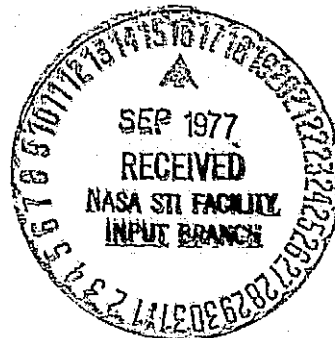
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1. INTRODUCTION

The purpose of this program was the development of three identical 12 GHz to 2.6 GHz image and sum frequency enhanced mixer/local oscillator assemblies and one 12 GHz parametric amplifier. The mixer specifications have been derived on the basis that these units will provide a low cost method of converting the present low cost 2.6 GHz HET ground receivers to operate with the 12 GHz repeater to be flown on the Communication Technology Satellite. The parametric amplifier specifications have been derived on the basis that this unit would provide a low cost method of significantly improving the quality of performance (by lowering the overall noise figure) of 12 GHz ground receivers.

To realize the prime objective of low cost, it was proposed that an all solid state, microwave integrated circuit approach be pursued for both the paramp and the converter. This represented a radical departure from the conventional paramp approach which uses a coaxial signal circuit and packaged varactors embedded in a waveguide pump and idler circuit. For the converter, such an approach is conventional (at Westinghouse).

The effort with the converter was completely successful and state-of-the-art results were obtained. While, with the paramp, extreme difficulty was encountered in controlling the K_a -band idler and pump signals. The slot line circuits used were found to be extremely difficult to tune (match) and tended to radiate strongly. Thus this part of the effort was unsuccessful.

1.1 PROGRAM OBJECTIVES

The objectives of this program were outlined in the contract work statement entitled, "Development of a 12 GHz to 2.6 GHz Image and Sum Frequency Enhanced Mixer/Local Oscillator Assembly and a 12 GHz Parametric Amplifier," dated 28 February 1974.

Past development efforts for the 12 GHz front ends may be divided into three categories: parametric amplifiers to achieve noise figures below 3 dB, tunnel diode amplifiers to achieve noise figures around 6 dB and diode mixers to achieve noise figures in the range of 13 dB. Under a recently completed contract (NAS 5-21845) a low noise figure, low conversion loss 12 GHz image and sum frequency enhanced mixer was successfully developed. This effort demonstrated the feasibility of achieving high performance at low cost. This has been made possible by the significant advances over the past several years in device and manufacturing techniques.

It was an objective of this effort to apply the design principles of the previous contract (NAS 5-21845) to develop and demonstrate the feasibility of a low cost 12 GHz to 2.6 GHz image and sum frequency enhanced mixer/local oscillator assembly to convert existing 2.6 GHz HET ground receivers to operate with the CTS.

The development of 12 GHz parametric amplifiers achieving less than 3 dB noise figures has been carried out in the past. The significant feature of the subject effort is the potential of low cost.

Under a now completed contract with the U. S. Army Electronics Command (Contract DAABO7-72-CO221), Westinghouse had under development a parametric amplifier with the potential for high-volume low-cost production through the use of such integrated circuit techniques as microstrip trans-

mission lines, drop-in circulators, diode chips, coplanar and slot transmission lines.

Low noise figure performance was achieved by the use of contractor-developed Gallium Arsenide Schottky Barrier varactor diodes with the highest cut-off frequencies available at this time, and because of the low insertion loss properties of the integrated circuit elements mentioned above.

It appeared, therefore, possible to achieve high performance at low cost because of the significant advances made over the past several years in manufacturing, circuit implementation, materials processing and semiconductor technology.

It was the objective of this effort to carry-over to the present development, the design principles and therefore the same desirable features and performance of the above mentioned contract, and to thereby develop and demonstrate the feasibility of producing low cost 12 GHz parametric amplifiers for use with certain CTS ground receivers.

The scope of this effort is limited to the design, development, fabrication and testing of an integrated mixer and solid state local oscillator assembly and a parametric amplifier.

1.2 PROGRAM REQUIREMENTS

Westinghouse is to provide the necessary personnel, services, facilities, and materials to design, develop, fabricate, and test three (3) integrated image and sum frequency enhanced mixer/local oscillator converter assemblies. An auxiliary IF output will be provided at 2.2 GHz to accommodate a beacon signal whose RF frequency is 11.7 GHz. Since this frequency may be outside of the frequency range in which image enhancement occurs, the conversion loss associated with it will be greater than that for the principal signal band.

Westinghouse shall provide the necessary personnel, services, facilities, and materials to design, develop, fabricate, and test one (1) integrated parametric amplifier.

1.2.1 Performance Parameters

The performance parameters of the converters and the amplifier are listed in the following tables in terms of proposed design goals and contract specifications. The design goal represents performance considered to be theoretically realizable; that is, can be analytically justified and achieved by utilization of components and technology already within the state-of-the-art or by a reasonable extension thereof.

TABLE 1-1: PERFORMANCE PARAMETERS - CONVERTERS

| <u>Parameter</u> | <u>Design Goal</u> | <u>Specification</u> |
|--|--------------------|----------------------|
| RF Signal Frequency Band | 11.7 to 12.2 GHz | 12.0 to 12.15 GHz |
| IF Signal Frequency Band | | 2.5 to 2.7 GHz |
| LO Frequency | | 9.486 GHz |
| Beacon Frequency | | 11.7 GHz |
| Input/Output Impedance | | 50 ohms |
| RF Return Loss Band for 13 dB min. | 11.7 to 12.2 GHz | 12.0 to 12.15 GHz |
| IF Return Loss Over 2.5 - 2.7 GHz Band | > 10 dB | |
| Signal Band Conversion Loss | | |
| Over 12.0 to 12.15 GHz Band | | < 4.0 dB |
| Over 11.7 to 12.2 GHz Band | < 3.5 dB | |
| Beacon Frequency Conversion Loss | < 5.0 dB | < 6.0 dB |
| Mixer Noise Ratio Over 11.7 to 12.2 GHz Band | ≈ 1.0 | |

TABLE 1-1: (Continued)

| <u>Parameter</u> | <u>Design Goal</u> | <u>Specification</u> |
|--|--------------------|-------------------------|
| Mixer Noise Figure | | |
| Over 12.00 to 12.15 GHz Band | | < 4.0 dB |
| Over 11.7 to 12.2 GHz Band | < 3.5 dB | |
| Local Oscillator Frequency Stability | | \pm 1 MHz per 8 hours |
| Amplitude Linearity | | |
| Design goal such that third order intermodulation products are better than 30 dB below the desired signal when two -55 dB carriers are applied simultaneously. | | |
| Environment: The unit shall meet the electrical requirements over the temperature range of -50°C to $+60^{\circ}\text{C}$. | | |

TABLE 1-2: PERFORMANCE PARAMETERS - PARAMETRIC AMPLIFIER

| <u>Parameter</u> | <u>Design Goal</u> | <u>Specification</u> |
|--|--------------------|----------------------|
| RF Signal Frequency Band | 11.7 to 12.2 GHz | 11.85 to 12.15 GHz |
| Input/Output Impedance | | 50 ohms |
| Input/Output VSWR over 11.85 to 12.15 GHz Band | | $\leq 1.5:1$ |
| Gain over 11.85 to 12.15 GHz Band | | ≥ 15 dB |
| Noise Figure over 11.85 to 12.15 GHz Band | < 2.5 dB | |
| Amplitude Linearity | 3.0 dB | |
| Design goal such that third order intermodulation products are better than 30 dB below the desired signals when two -55 dBm carriers are applied simultaneously. | | |

2. TECHNICAL DISCUSSION

To be described in the following sections are the 12 GHz to 2.6 GHz converter and the 12 GHz paramp development effort. The converter material includes the theory of the image and sum frequency enhanced mixers, the local oscillator development and the converter performance. The paramp material includes a description of the paramp components developed, the paramp design details, and the limited results obtained.

Both units are of hybrid (truly integrated) form. They contain distributed element microstrip ferrite circulators, microstrip transmission lines and filters, distributed terminations, microstrip signal impedance transformers, coplanar-slot line hybrid junctions for balanced semiconductor diode modulation (in the mixer and in the paramp), broadband transitions from slot line to microstrip, and high Q radial and waveguide cavities for the solid state oscillators.

2.1 CONVERTERS

The converter is made up of a high performance mixer and very stable local oscillator.

The mixer is a broadband, low conversion loss, image enhanced, balanced mixer. It is a unique design, comprising microstrip, slot line, and coplanar transmission lines with a slot line, coupled microstrip type of image reject signal bandpass filter and microstrip directional filters for LO insertion and IF beacon signal separation.

The local oscillator uses a Gunn diode active element for minimum LO noise and uses a temperature compensated high Q rectangular waveguide cavity to obtain the high Q necessary for LO frequency stability and spectral purity.

2.1.1 Mixer Analysis

The techniques for the enhancement of mixer operation by the control of the terminal impedances at the image frequency and higher order mixing products are well known and described in the literature¹⁻⁸. The frequencies of importance are the modulation products which exist according to the heterodyne principle by which the mixer operates. The received signal (RF), together with a higher level signal from a local oscillator (LO), are applied to a nonlinear element.

If the RF signal is sufficiently small that the mixer can be considered distortion - free, then the resulting frequencies can be given as $f_n = nf_p + f_o$; $n = -\infty, \dots, +\infty$; where $f_o = |f_s - f_p|$ is the output (IF) frequency, f_s and f_p being the RF and LO frequencies, respectively. Note also that for the present application, $-f_{-1}$ corresponds to the signal frequency, and f_{+1} to the conventionally designated image frequency. This frequency spectrum is shown in Figure 2-1. For most mixer applications $f_o \ll f_p$, thus this notation has the advantage that $|f_n| \approx f_{+n} \approx nf_p$; $n = 1, \dots, +\infty$; and the magnitude of the frequency is readily identifiable by its subscript. Further, for a particular group about nf_p , the plus (+) subscript always refers to the upper sideband and the negative (-) subscript always refers to the lower sideband. The three frequencies at the n^{th} level are sometime referred to as the n^{th} order idler frequencies.

The loss in converting an RF signal to an IF signal depends not only on properly matching the RF and IF impedances, but also upon properly termina-

ting the sum and image frequencies as well as various other idler frequencies⁷. Equally as important as proper signal termination is the attainment of the proper form of mixer modulation by the LO.

Saleh⁷ has given about the most comprehensive treatment, to date, of the theory of resistive mixers. He introduced and gave the methods of analysis of four basic resistive mixers; the Z-, Y-, H-, and G-mixers. The names originated from the types of network matrices that had to be used to find the mixer performance. The Z-mixer is obtained by open-circuiting all the out-of-band frequencies and the Y-mixer is obtained by short-circuiting the out-of-band frequencies. For the H- and G-mixers, the out-of-band frequencies were divided into two groups; the odd- and even-ordered idlers. The H-mixer is obtained by open-circuiting the odd-ordered idlers and short-circuiting the even-ordered idlers. The G-mixer is the dual of the H-mixer.

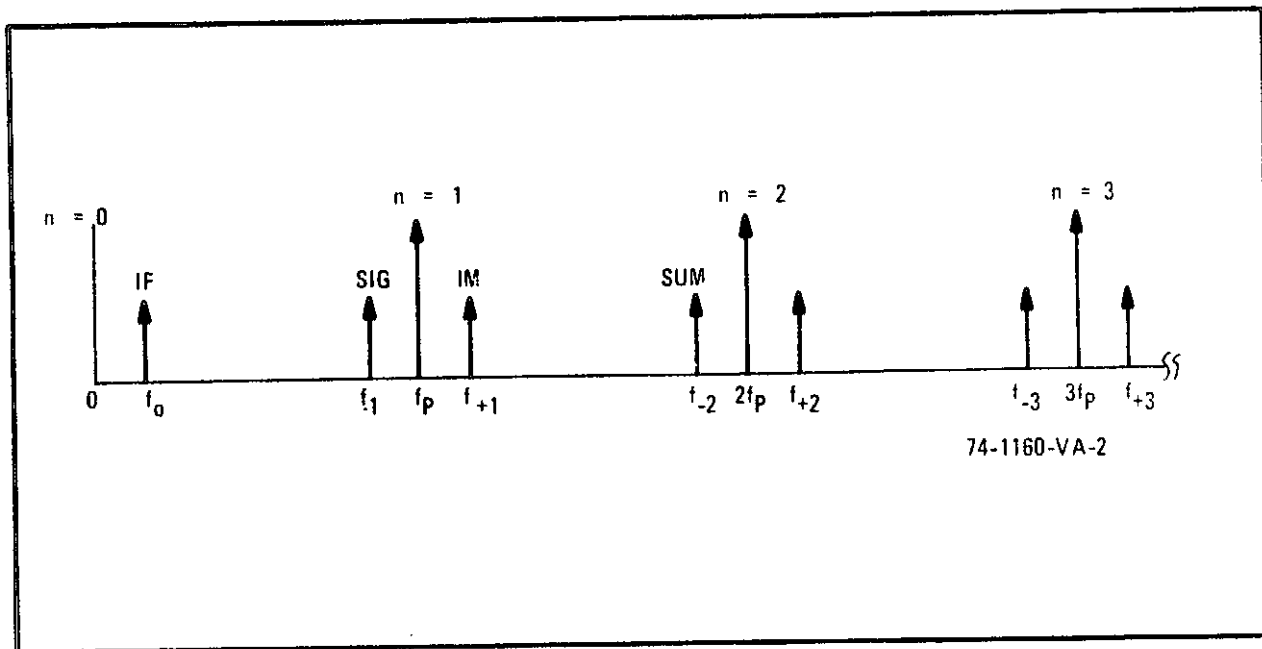


Figure 2-1: Frequency Spectrum, $|f|$, of Mixer with LO (f_p) and RF Signal (f_{-1}).

It was shown that, in a mixer without limiting parasitics, the lowest theoretically attainable conversion loss is obtained with a symmetrical rectangular LO drive waveform and dual terminations at the even and odd idler frequencies (that is, open circuits for the even and short circuits for the odd idlers or vice versa). These are the G- and H-type mixers.

In practical cases, mixer diodes are not purely resistive. The diode parasitics play an important role in the determination of the type of mixer to be used and the type of analysis that applies. It can be shown that by adding a fixed or time varying reactance in parallel with the variable resistance in a Y-mixer or in series with the variable resistance in a Z-mixer, one can find a closed form solution for the mixer equations. The diode junction capacitance and series resistance represent the known diode parasitics. In the literature are found many authors who have dealt with this problem in Y-mixers. These authors assumed that the junction capacitance short circuits across the variable resistance all the higher order out-of-band frequencies. Thus, only the signal, IF, and the image frequency voltages were considered. This assumption reduced the Y-mixer equations to a complex 3 x 3 Y-matrix which could be easily handled.

Barber⁴ has presented such an analysis of microwave Y-type mixers wherein it was shown that the pulse duty ratio of the Schottky diode current waveform was the most fundamental parameter for defining mixer operation. It can be shown that most microwave mixer diodes behave as though the barrier itself were switched on and off at the LO rate; and that the resistance in the ON state is just that of the limiting series resistance (R_s), and the impedance in the OFF state is just that expected of the series resistance, R_s , in series with the barrier capacitance, C_j . Of course the barrier capacitance

is a function of voltage and time, but good correlation with measured results is obtained if the zero bias capacitance value is used. Thus, a cutoff frequency, $f_{co} = (2\pi R_S C_j)^{-1}$, may be defined to which the circuit losses may be related.

Using these considerations, an extension of Barber's analysis^{9,10} has allowed the calculation of the conversion loss as a function of the pulse duty ratio and as limited by the operating frequency to cutoff frequency ratio (f/f_{co}). Figure 2-2 shows the expected mixer conversion loss that would be obtained for the broadband case (wherein the image termination equals the signal termination). Figure 2-3 shows the computed mixer conversion loss for the case wherein the image is short-circuited.

Figures 2-4, 2-5, and 2-6 show the computed values of mixer terminal impedances plotted as functions of the pulse duty ratio (t). In each case, the RF signal impedance, R_{RF} , has been chosen to minimize the mixer noise figure. This condition also results in an input impedance match. The RF and IF impedances have been computed as quantities normalized to R_O . R_O is the average diode impedance and is well approximated by the simple expression

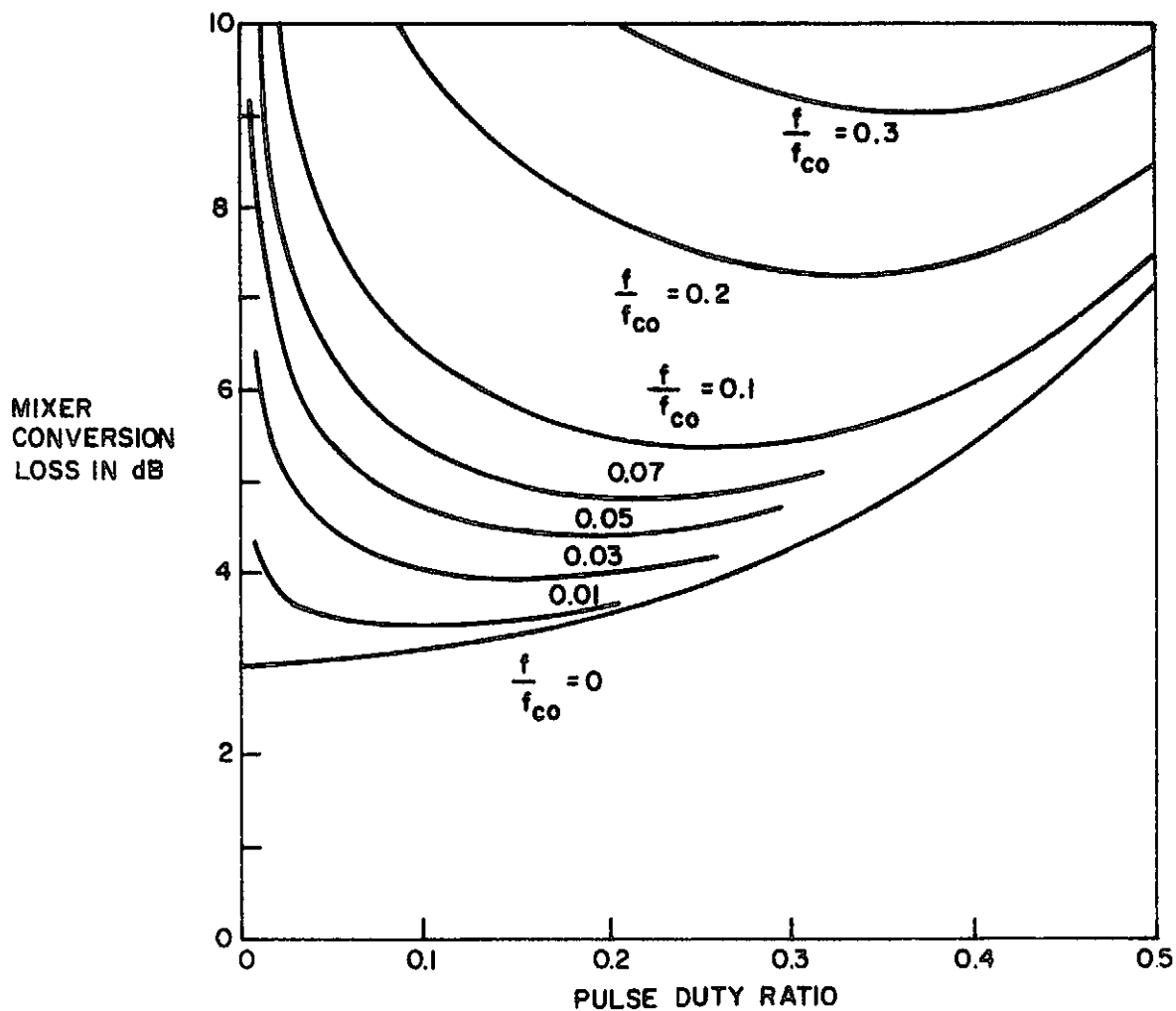
$$R_O = \frac{R_S}{t} \quad (2-1)$$

This is the time averaged diode impedance and thus is the impedance presented to the LO.

The rectified dc current is a useful quantity for checking mixer operation and can be calculated by using equation (2-2).

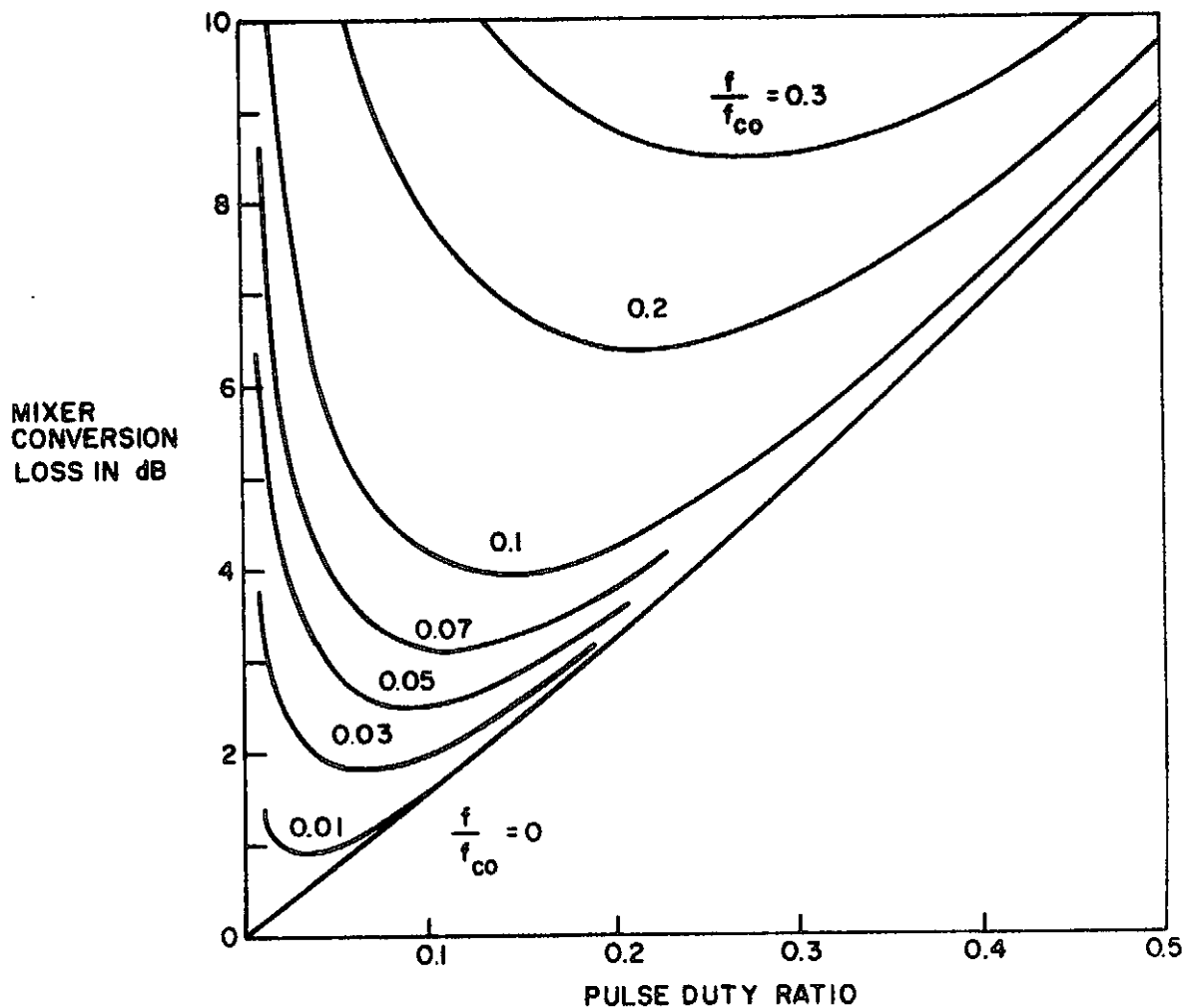
$$I_{dc} \cong \left(\frac{Pt}{R_S}\right)^{\frac{1}{2}} \left[\frac{.9 \sin(\pi t) - \sqrt{2} t \cos(\pi t)}{1 + t} \right] \quad (2-2)$$

where P is the LO power, t the pulse duty ratio, and R_S the diode limiting resistance.



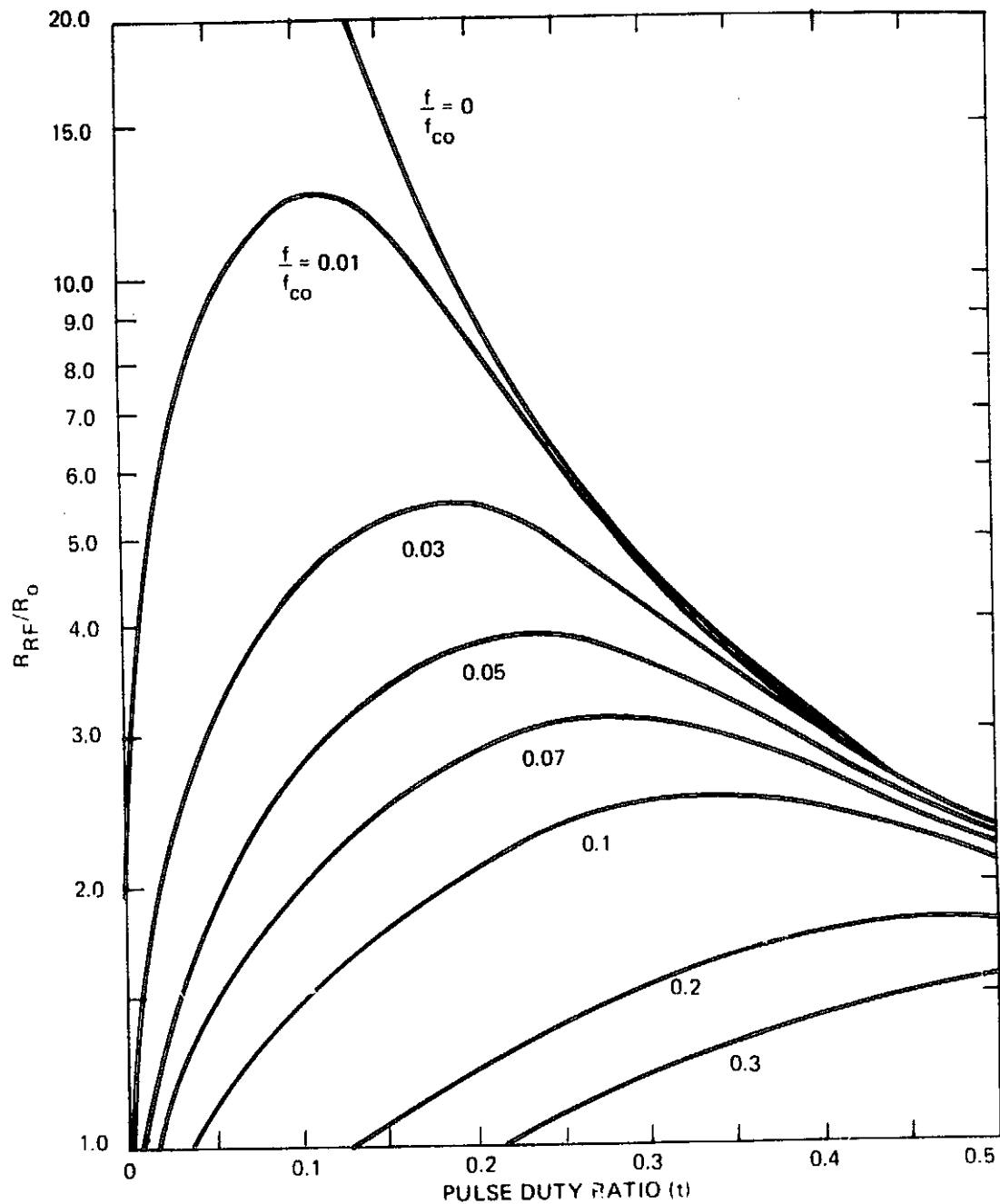
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Figure 2-2: Computed Mixer Conversion Loss for the Broadband Case (Image Termination Equals Signal Termination)



S73-0206-VA-4

Figure 2-3: Computed Mixer Conversion Loss for Short-Circuited Image Case



S-73-0765-V-8

Figure 2-4: Computed RF Impedance for the Broadband Case

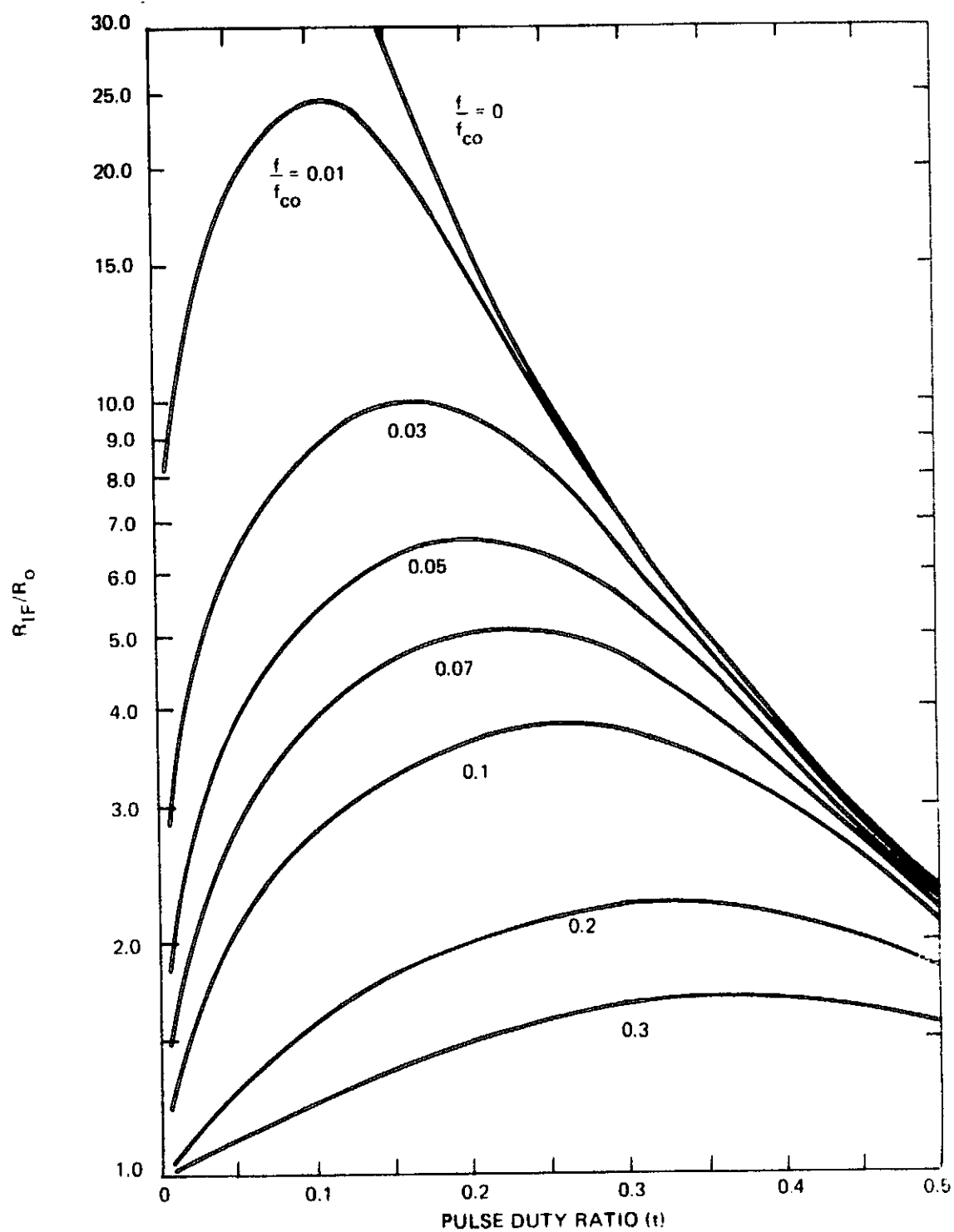
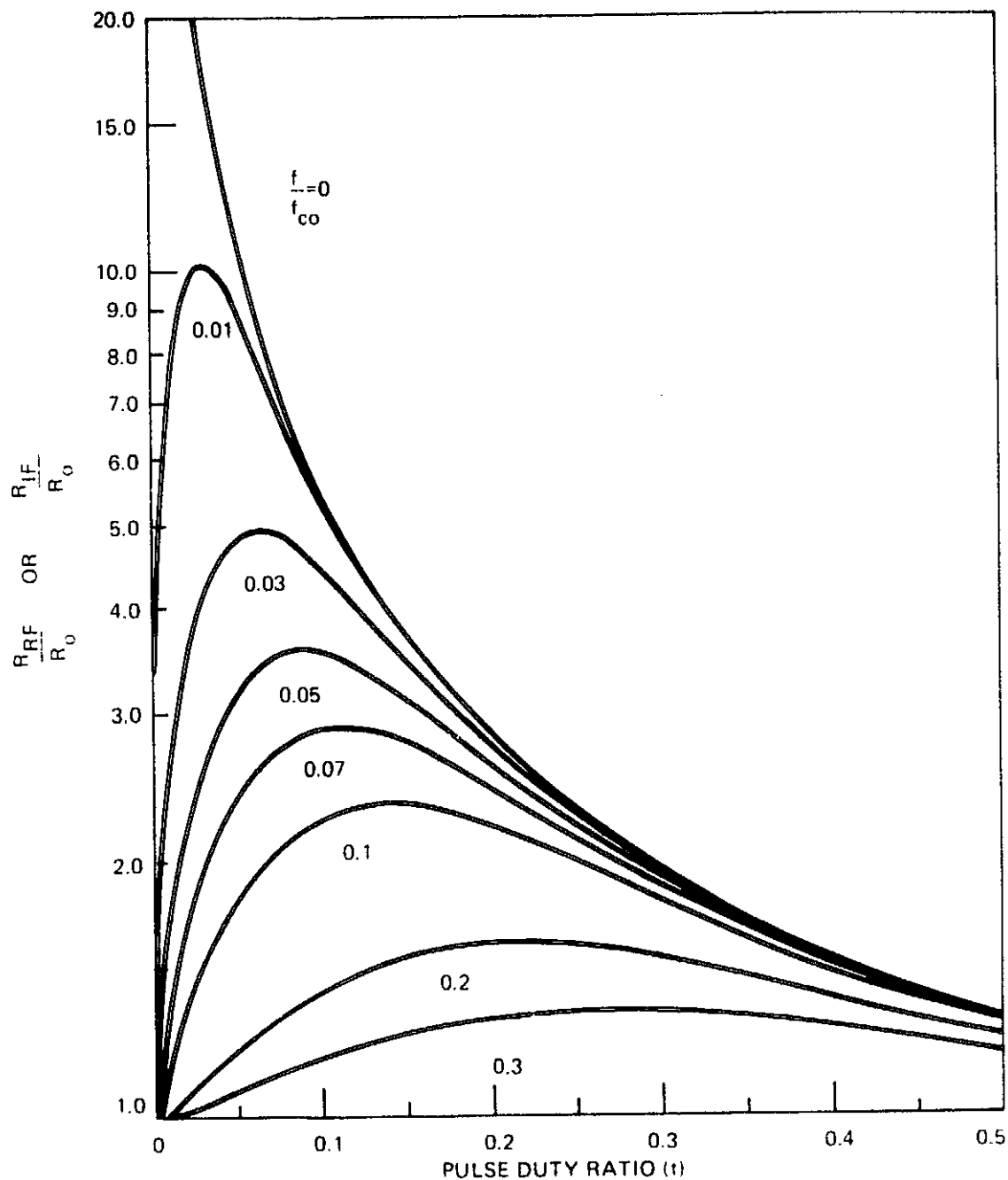


Figure 2-5: Computed IF Impedance for the Broadband Case



S-73-0765-V-10

Figure 2-6: Computed Terminal Impedance for Case with Image Short-Circuited

The local oscillator power can be estimated by equation (2-3).

$$P = \frac{t (V_o - V_b)^2}{R_s [1 + \cos(2\pi t)]} \quad (2-3)$$

where V_o is the forward potential drop of the Schottky barrier, and V_b is the bias voltage. Typical values for V_o are 0.75 V (GaAs), 0.5 V (Si-Schottky barrier), and 0.15 V (Si-point contact).

2.1.2 Mixer Design

Image enhanced mixers can yield substantial improvement in performance only if high performance diodes are available. The measure of potential performance is indicated by the frequency cutoff of the diode. Very high frequency cutoff (f_{co}) is required for low conversion loss. Until the advent of the Schottky barrier diode, and in particular, the GaAs Schottky barrier, sufficiently high f_{co} diodes were not available and image enhanced mixers were only an academic curiosity. Now such Schottky barriers are readily available and low conversion loss mixers are a reality.

2.1.2.1 Schottky Barrier Junction Properties

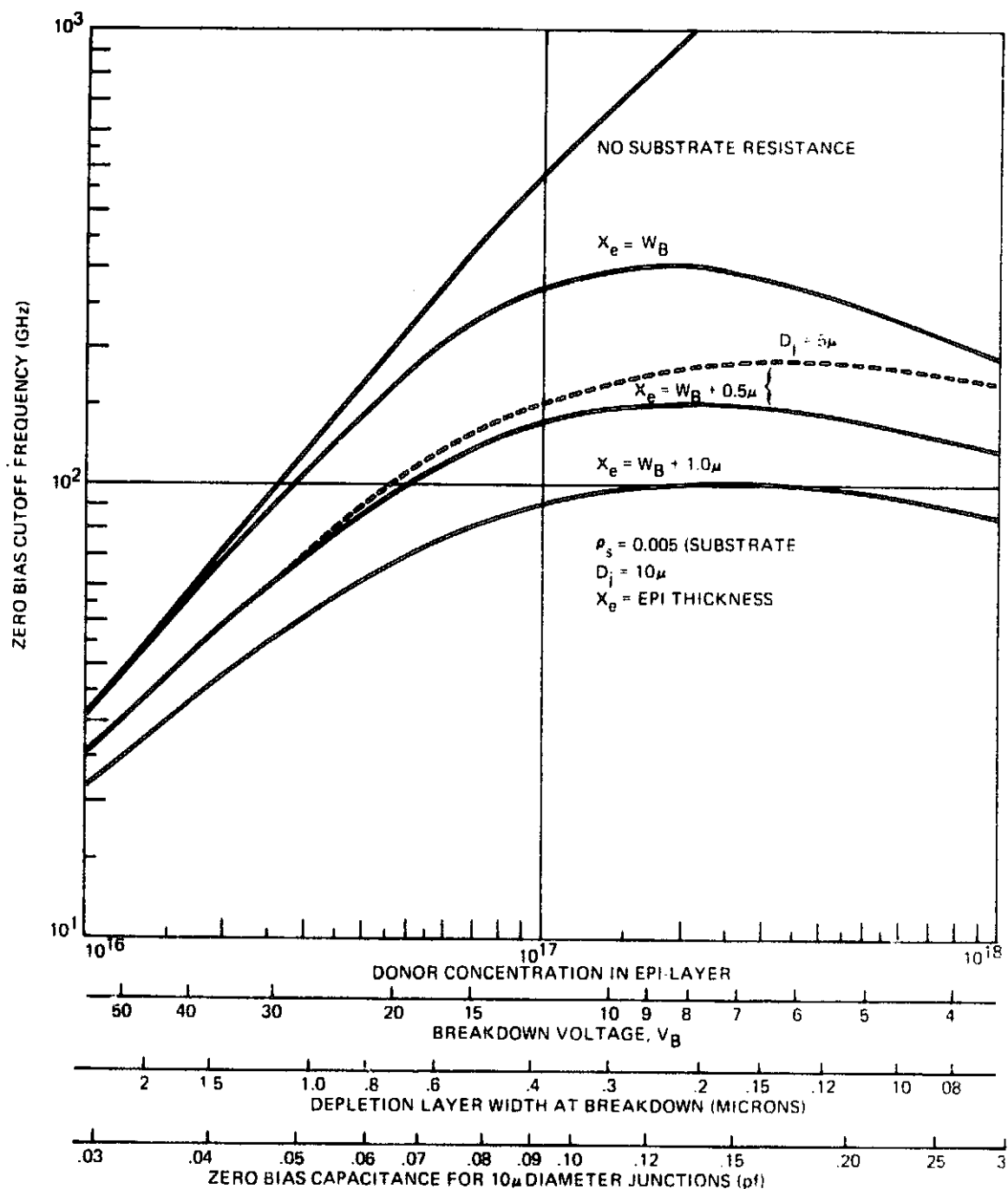
The Schottky barrier used for mixers primarily requires the variable resistance property of a junction, thus it is commonly called a varistor. The variation of resistance of a varistor as a function of applied voltage is dramatic. The reverse bias resistance is of the order of many megohms. The resistance decreases rapidly with increasing forward bias until the forward bias series resistance, R_s , dominates over the effect of the junction resistance.

The junction resistance is in parallel with a junction capacitance, C_j , which is also a voltage variable component. The varistor must be designed such that the junction capacitance is minimized for a given series-limiting

resistance. To compare varistors of differing R_s and C_j values, it is useful to define a cutoff frequency, $f_{co} = (2\pi C_j R_s)^{-1}$. For this comparison, the zero bias value for f_{co} is useful. It has been found that this value correlates well with measured results.

Figures 2-7 and 2-8 show the f_{co} as computed for silicon and GaAs Schottky barriers. The value for R_s is made up of two parts. The first is the resistance of the epitaxial region, X_e ; and the second is the parasitic resistance due to the spreading of the current from the epitaxial layer into a substrate of finite conductivity, ρ_s . Two values of junction diameter, D_j , were assumed. Three values of X_e were assumed. The first curve shows the limiting value of f_{co} due to the junction alone (no substrate resistance) and the epi-layer thickness is taken to be $X_e = W_B$. The remaining curves assumed a substrate spreading resistance. The second curve was calculated assuming the epitaxial layer thickness, X_e , to be just enough to accommodate the space charge region at breakdown, W_B . The third and fourth curves make an allowance in the epi-layer thickness of 0.5μ and 1.0μ respectively.

The effect of the parasitic substrate resistance is clearly apparent in the figures, both in the drastically reduced f_{co} and in the occurrence of a maximum in the curves. The breakdown voltage-impurity density relationship of Sze and Gibbons¹¹ for an abrupt junction has been plotted also in the figures. These breakdown voltages represent bulk breakdown characteristics. Note that the f_{co} calculation has been made assuming at least an epi-thickness sufficient to be fully depleted at breakdown. This allows maximum breakdown voltage for a given doping level. If a much reduced epi-thickness is used, then an improvement in f_{co} can be obtained. Assume a GaAs epi-layer doping of 10^{16} , and a thickness of 0.5μ . Then one can calculate an f_{co} (for the



S 73-0765-V-6

Figure 2-7: Theoretical Parameters of Epitaxial Silicon Schottky Barriers

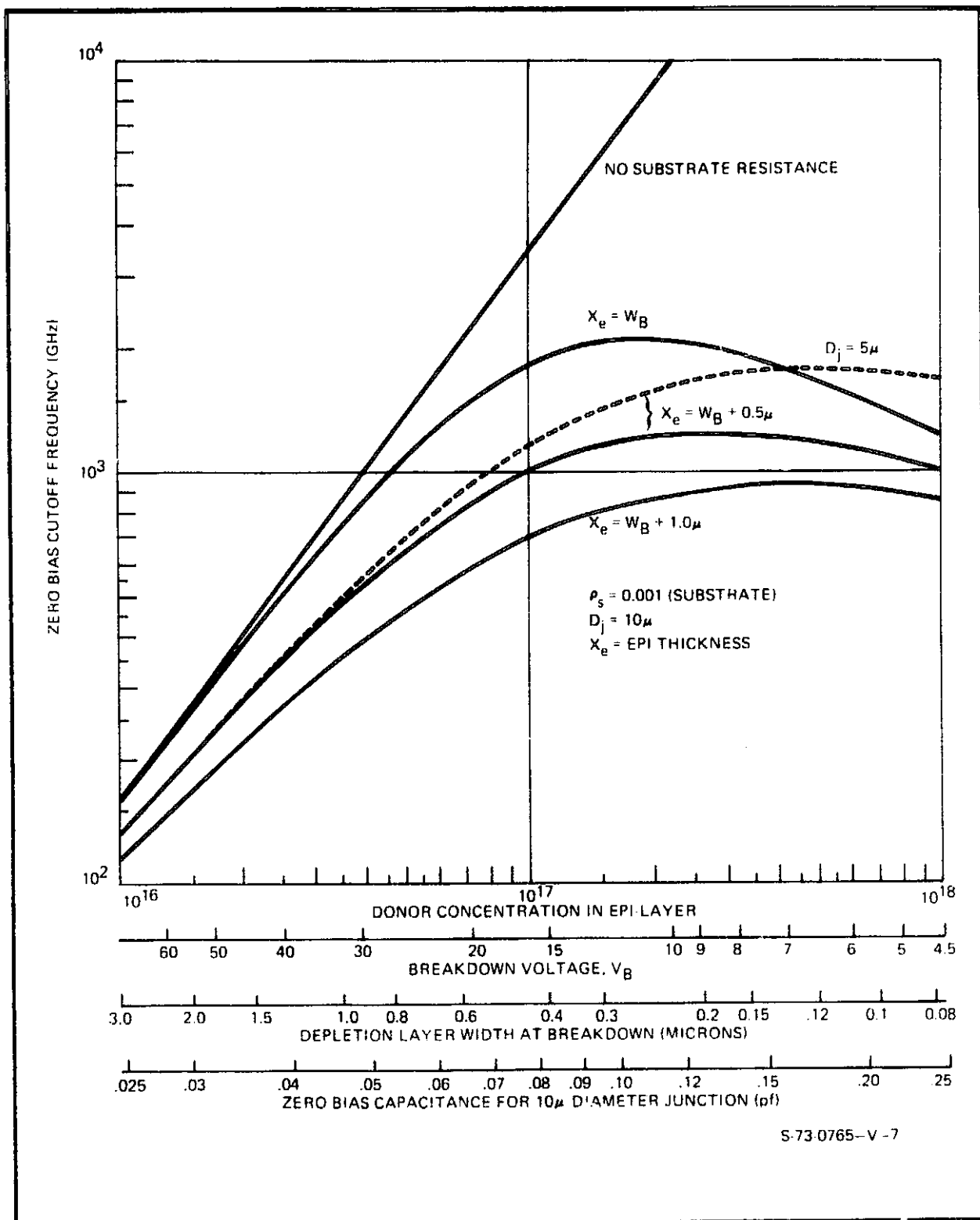


Figure 2-8: Theoretical Parameters of Epitaxial GaAs Schottky Barriers

10 μ diameter junction on GaAs) of 2,283 GHz, a breakdown voltage of 22 volts, and a punchthrough voltage of 2.0 volts. The zero bias capacitance is 0.024 pF. Now suppose that an excess of 0.5 μ were left on this epilayer (due to processing variables). Now the value for f_{co} drops to 604 GHz, a drastic change in the value for R_s . Thus the epilayer thickness for this diode becomes an extremely critical control parameter. However, such a thin layer diode is attractive, especially for high burnout diodes because, for a given application, a junction diameter of 20 μ on a 0.5 μ epilayer of 10^{16} will give about the same impedance level and f_{co} as a junction diameter of 10 μ on a 0.5 μ epilayer of 2×10^{17} . Such diode would have a two-to-one thermal impedance improvement over the smaller diode. The case for which the barrier depletion layer at zero bias extends through, or nearly through, the entire lightly doped epilayer represents a special form of metal-semiconductor barrier known as a Mott barrier³.

Note in Figures 2-7 and 2-8 that there is an order of magnitude difference in the f_{co} scales between Si and GaAs. Realistic substrate resistances have been assumed. It can be seen that if one assumes a nominal 0.5 μ excess of epilayer material for both Si and GaAs, that for 10 μ junctions, the Si devices will yield an f_{co} of no more than 150 GHz; the GaAs devices can be expected with f_{co} on the order of 1,000 GHz. These numbers are realistic and have been readily approximated in practice. Thus GaAs is the natural choice for very low conversion loss mixers.

2.1.2.2 Design Configuration

Figure 2-9 shows the implemented design which allows complete realization of the desired image-enhanced balanced mixer using GaAs Schottky barrier diode. This is a plan view of the MIC mixer as viewed from the microstrip track side of the alumina substrate. Figure 2-10 is a more detailed sketch of

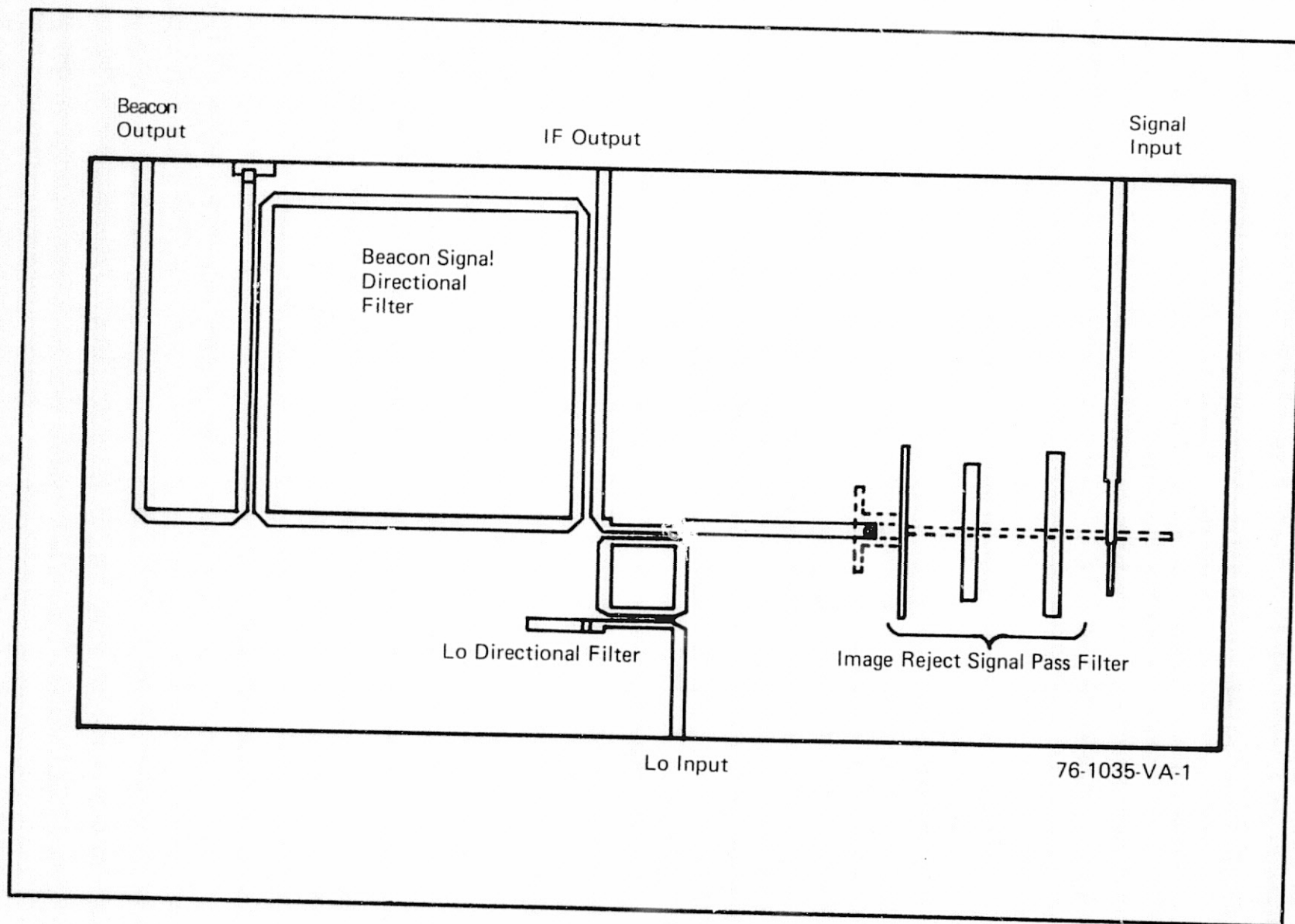


Figure 2-9. Image Enhanced Balanced Mixer MIC Board Layout

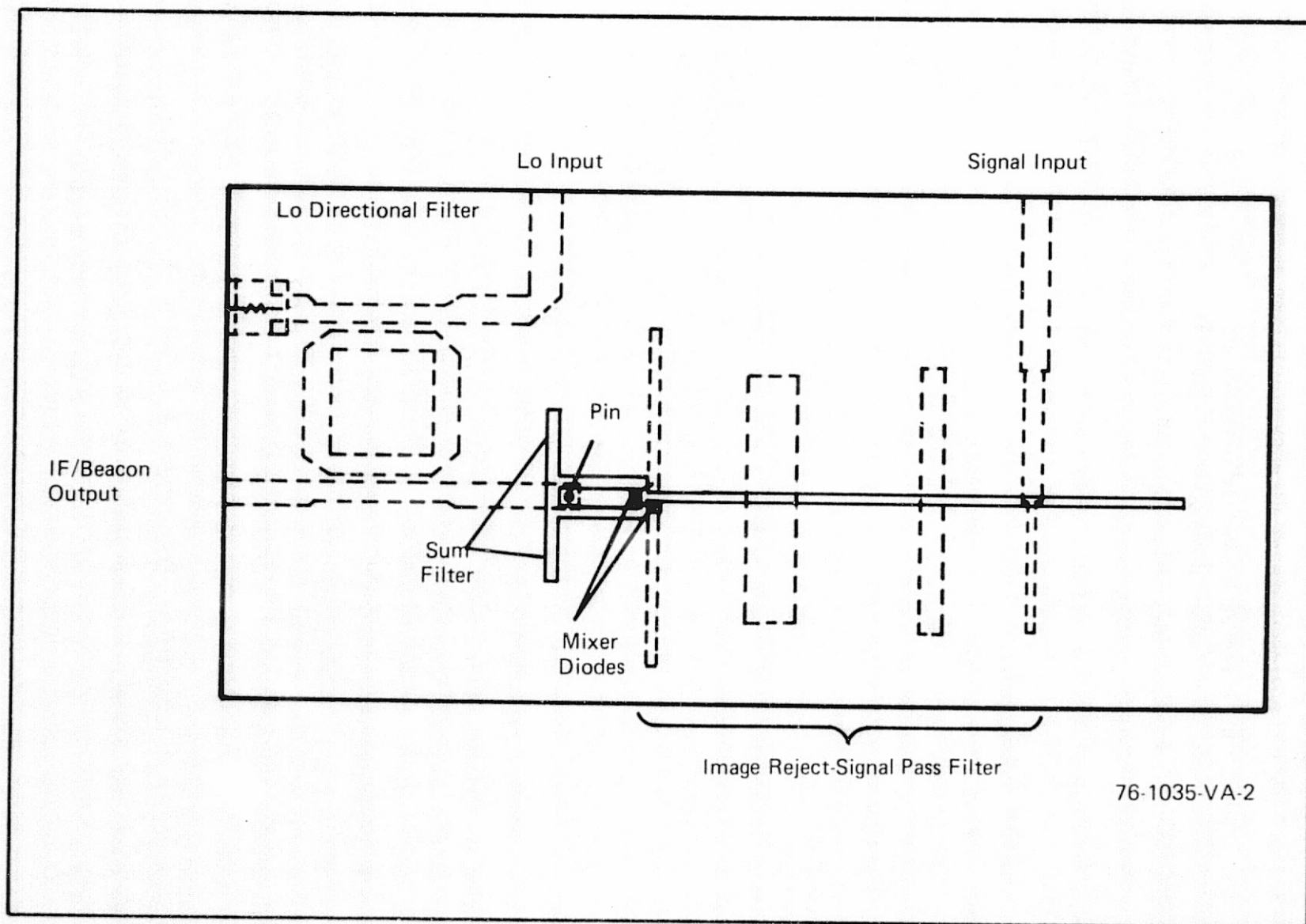


Figure 2-10. More Detailed MIC Board Layout

the mixer but with the beacon signal directional filter removed. Figure 2-10 is a plan view of the mixer as viewed from the ground plane side of the alumina substrate.

The RF signal at nominally 12 GHz enters the substrate on the right top edge via the microstrip (signal input) port. The RF is coupled to the diodes via a broadband microstrip to slot line transition and through a signal bandpass, image reject, impedance matching filter consisting of microstrip lines coupled to the slot line. The pair of mixer diodes terminate this filter.

The LO at a frequency of 9.5 GHz is injected via the LO input microstrip terminal. The LO power then passes through the directional filter and to the mixer diodes by way of a microstrip to coplanar line transition (pin through the substrate). Slot line stubs at the end of the coplanar line section present a short circuit to the mixer diodes at the sum frequency. The diodes are arranged so that the IF/Beacon output line is common with the LO input. The wide frequency separation of the IF and LO, and the directional and frequency selective properties of the directional filter allow very simple diplexing of the two signals with essentially zero bandwidth limiting of the IF port. As is seen in Figure 2-9, a second narrow band directional filter is used to separate the beacon signal from the main IF band.

The two diodes are in parallel to the IF and LO ports, but in series to the signal port. As the conventional IF amplifier input impedance is nominally 50 ohms, the microstrip-coplanar line characteristic impedance is set to 50 ohms. In a short-circuited image mixer, the signal impedance is equal to the IF impedance. Thus the diode impedance must be 100 ohms, the two in parallel then matching the 50-ohm line. But the two in series will present 200 ohms to

the signal slot line. The slot line can readily be made with a characteristic impedance of nominally 100 ohms. The 50-ohm microstrip to 100-ohm slot line transition has well in excess of 10 percent bandwidth. The signal filter then is designed to supply the impedance transformation required to match the 200-ohm diode impedance to the 100-ohm slot line impedance.

Reference to Figure 2-3 will show that a conversion loss of under 2.0 dB can be achieved with diodes of $f_{co} = 800$ GHz and with $PDR = 0.10$. The signal load impedance, R_{RF} , can be obtained from Figure 2-6, and is found to be $R_{RF} = 5.5 R_o$. The impedance to the LO port is given by equation 2-1. So that if $R_{RF} = 100$ ohms, and $t = 0.10$, then $R_{LO} = 18.0$ ohms. The LO line will then have a VSWR = 5.5:1.

Using equation 2-1, and the fact that $R_{RF} = 100$ ohms, one finds $R_s = 1.8$ ohms for $t = 0.10$. Assuming a diode frequency cut-off of 800 GHz, the junction capacitance is found to be $C_j = 0.11$ pF. A junction diameter of about 10 microns will yield this value of C_j with an attendant $f_{co} = 800$ GHz.

A computer program has been written which allows the analysis and optimization of microwave circuits with embedded mixer diodes. The diode model used was that which assumes that the Schottky diode can be represented as a junction switched at the LO rate. In the ON condition, the resistance is that of the limiting series resistance; and in the OFF state, it is the series resistance in series with the barrier capacitance. The zero bias capacitance was used for the analysis and appears to give good correlation with measured results. In this computer routine a three frequency analysis is used. That is, the diodes are represented by black boxes with terminals at the RF, IF and image frequencies with couplings set by the 3×3 conductance matrix. All other frequencies generated are assumed to be shortcircuited. A nodal analysis

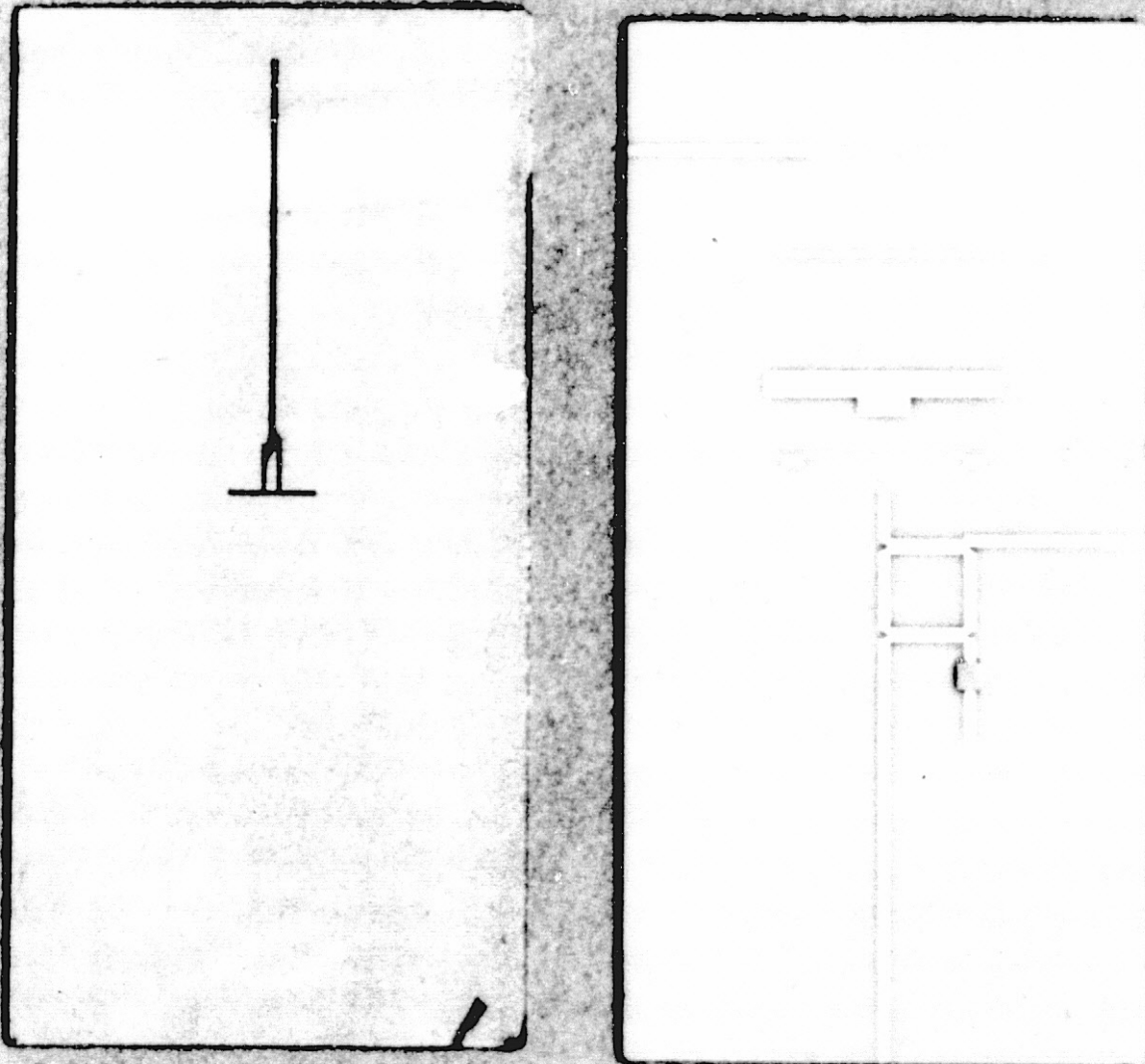
routine is used to model the external circuitry at the three frequencies of interest and the diodes are added in parallel. An optimization program is then used to vary circuit values until the desired results are obtained. The computer results tracked the measured values within 0.4 dB over the band.

The signal filter loss was estimated to be ≈ 1.0 dB. The conversion loss was $L_c \approx 1.6$ dB. The microstrip to slot line transition is no more than 0.25 dB, so that an overall conversion loss for the complete mixer should be about 2.85 dB. An additional loss of about 0.3 dB must be added for the 3-mm coaxial connectors used to bring in the RF input signal and to remove the IF. Because of the beacon coupler, the IF signal encounters an additional 0.5 dB of loss. Thus the total conversion loss (band center) is expected to be about 3.65 dB.

An estimate for the L_o power is obtained from equation 2-3. It is obvious by inspection of Figure 2-10 that the diodes are dc short-circuited and thus $V_b = 0$. For the GaAs devices being used, $V_o \approx 0.75$ volt. Thus, for the diode with $R_s = 1.8$ ohms, and an L_o power of about 17 mW is required to attain the $PDR = 0.1$. As two diodes are being used, an available L_o power of ≈ 35 mW is required for full modulation and attainment of reasonable impedance levels.

Figure 2-11 is a photograph of the initial mixer (similar to Figure 2-10) and without the beacon directional filter. The photograph shows the substrate with diodes mounted (top and bottom views of the substrate). Figure 2-12 is a photograph of the final mixer actually used in the converter. Again, both top and bottom views are shown. Note the relatively large size of the beacon directional filter. The directional filter causes losses of about 0.5 dB to the main IF signal. The center frequency of the filter is somewhat lower than the beacon at 11.7 and the coupling to the main line is as light as

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Figure 2-11. Initial Mixer Without Beacon Directional Filter

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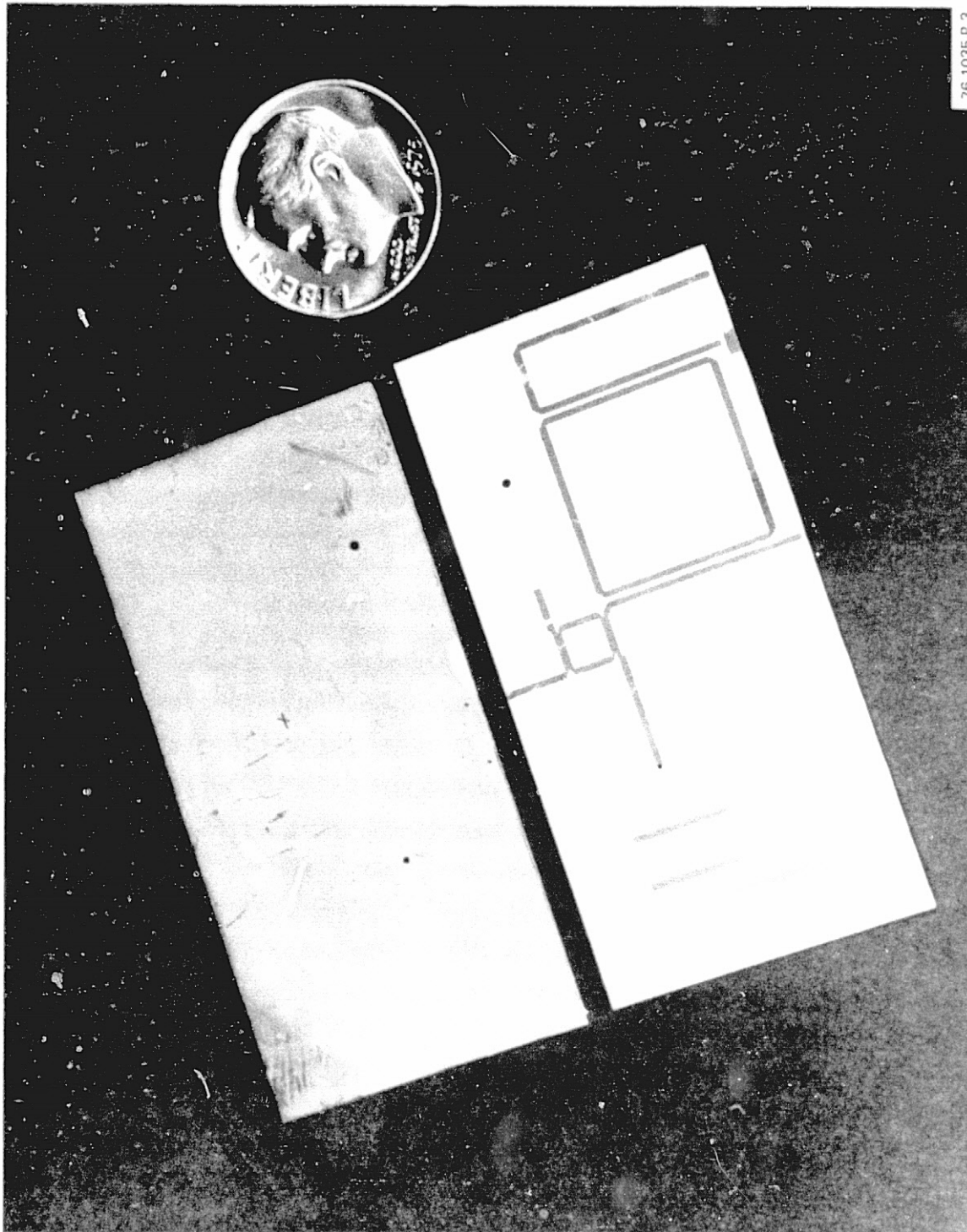


Figure 2-12, Final Design MIC Image Enhanced Mixer

possible to keep the IF signal losses to a minimum. This all causes directional filter loss at the beacon frequency of about 5 dB which then adds directly to the mixer conversion loss. Figure 2-13 shows the conversion loss vs frequency which is typical of the three delivered mixers. The conversion loss at the beacon frequency was about 8 dB on all three units. The data in Figure 2-13 represents all circuit losses including connector losses.

2.1.3 Local Oscillator Development

For the local oscillator (LO), a special high Q oscillator circuit was used with commercially available Gunn diodes and efficient means for coupling to microstrip without destroying the high Q of the oscillator circuit. The dc power is supplied to the Gunn diode by a stabilized regulator circuit.

A key feature of this oscillator is the stability of the oscillator frequency with temperature variations. No temperature stabilizer (heater) is used. A dielectric tuner inside a metal shaft is arranged in such a manner that the expansions of the cavity and tuner will compensate each other and result in frequency stabilization.

Cold temperature turn-on of the oscillator can sometimes be a problem. Operation at room temperature can be fully acceptable but as the temperature is lowered, say to -20°C , frequently oscillations will cease and output power drops to zero. This effect was encountered in this LO but was alleviated by the use of a transient over-voltage pulse applied to the Gunn diode at turn-on and temperature compensation of the supply voltage.

2.1.3.1 Local Oscillator Configuration

The circuit selected for use and which was highly successful was the iris coupled waveguide cavity to which the Gunn diode is post coupled.

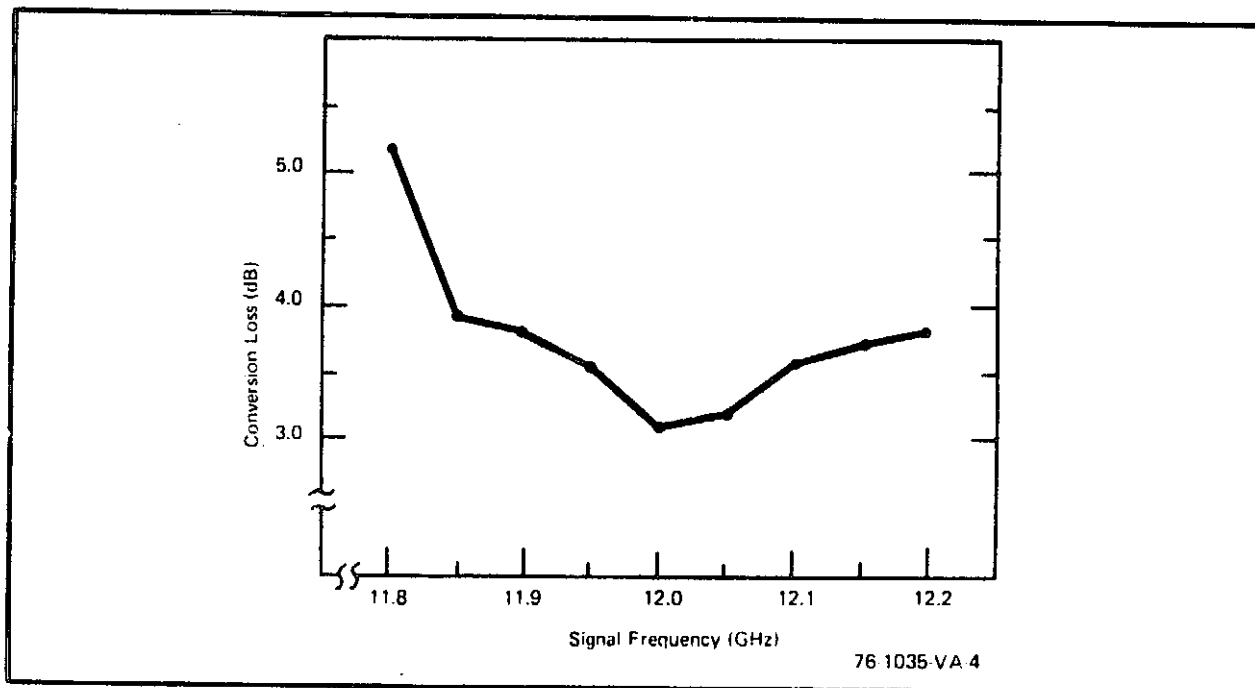


Figure 2-13. Conversion Loss Vs Frequency

This circuit has many features such as high stability, low FM noise, and low susceptibility to load pulling. The design of a single post/iris coupled cavity is relatively straight-forward for single frequency operation.

Figure 2-14 is a sketch of the iris coupled waveguide cavity oscillator. It is a section of rectangular X-band waveguide separated from the output waveguide by a coupling iris. The iris is simply a sheet of metal across the guide with a centrally located hole for coupling. The diode is mounted in the middle of a broad wall near the waveguide short circuit. The diode is post coupled to the waveguide. The bias circuits have been left out of Figure 2-14 for clarity.

The cavity operates in a TE₁₀₁ mode. The fundamental mode of this cavity is resonant when the distance from the iris to the effective waveguide

short position is a half wavelength. The effective short position, as shown in Figure 2-14, is somewhere between the diode post and the actual waveguide end wall.

A dielectric tuning rod located midway between the iris and the diode post serves as a smooth convenient method of tuning. The tuning rod could be either a low loss metal rod or a low loss high dielectric constant glass rod. The metal rod requires a good electrical contact with the cavity walls or a choke to prevent RF leakage. The glass rod has been chosen because it does not require a choke to prevent RF leakage. The only requirement of the glass rod is that its diameter be sufficiently small that there will be no coupling via the circular guide mode in the glass rod. The cutoff frequency for this circular waveguide mode is

$$f_c = \frac{6.92}{d\sqrt{K}} \quad (2-4)$$

where d is the diameter (in inches) of the tuner rod and K is the relative dielectric constant. In this design, a quartz rod is used to support a high dielectric constant glass tip which does the actual tuning. The quartz rod in the metal shaft is used for the frequency compensation. The quartz rod is 3/16 inch in diameter. The cut-off frequency for the waveguide mode in this rod is 18.5 GHz which is sufficiently far above the operating frequency as to cause no difficulty.

The coupling iris and output waveguide interact in such a way with the cavity as to determine the loaded Q of the cavity. The loaded Q can range from 40 to 4000; typical values being 100 - 200.

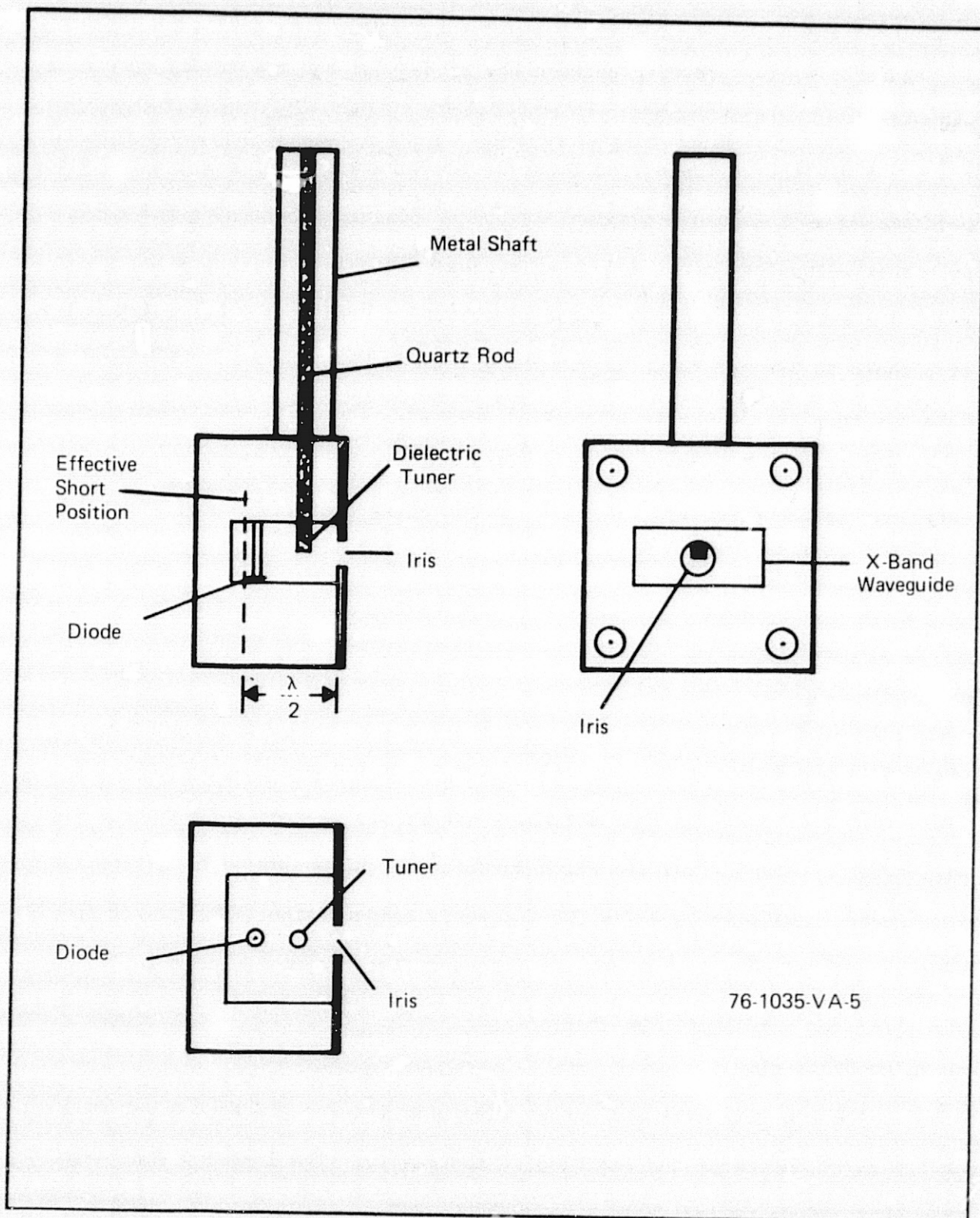


Figure 2-14. Iris Coupled Waveguide Cavity Oscillator

When the loaded Q (Q_L) is much smaller than the unloaded Q (Q_U), then Q_L of a simple half wavelength waveguide cavity can be estimated by the use of Figure 2-15 and equation 2-5.

$$Q_L \approx \frac{\pi}{2} \left(\frac{B}{Y_0} \right)^2 \left[1 - \left(\frac{f_c}{f} \right)^2 \right]^{-1} \quad (2-5)$$

where f_c is the cutoff frequency of the waveguide and (B/Y_0) is the susceptance of the iris as shown in Figure 2-15. Equation 2-5 has been evaluated for this design and the result is given in Figure 2-16. Therein is shown a curve of Q_L as a function of the iris diameter d . It was assumed that standard (0.9 x 0.4 inch) X-band waveguide is used for the cavity.

2.1.3.2 LO Temperature Compensation

In the present application, a very high degree of frequency stability is required. The specification is ± 1.0 MHz over the temperature range -50°C to $+60^\circ\text{C}$. The difficulty is shown by the fact that an aluminum cavity which has a coefficient of expansion of about 29 PPM/ $^\circ\text{C}$ will have a drift in the cavity resonance of about 348 kHz/ $^\circ\text{C}$. This is a 38 MHz drift over the required temperature range.

The temperature compensating scheme is shown in Figure 2-14. The dielectric tuner is epoxied to the end of a quartz rod. The rod is mounted inside a long metal shaft which expands with temperature. The rod and shaft are connected only near the top end of the shaft. As the shaft expands with increasing temperature, the tuner is withdrawn from the cavity. This tends to increase the frequency of cavity resonance, while cavity expansion tends to reduce the frequency of the cavity resonance.

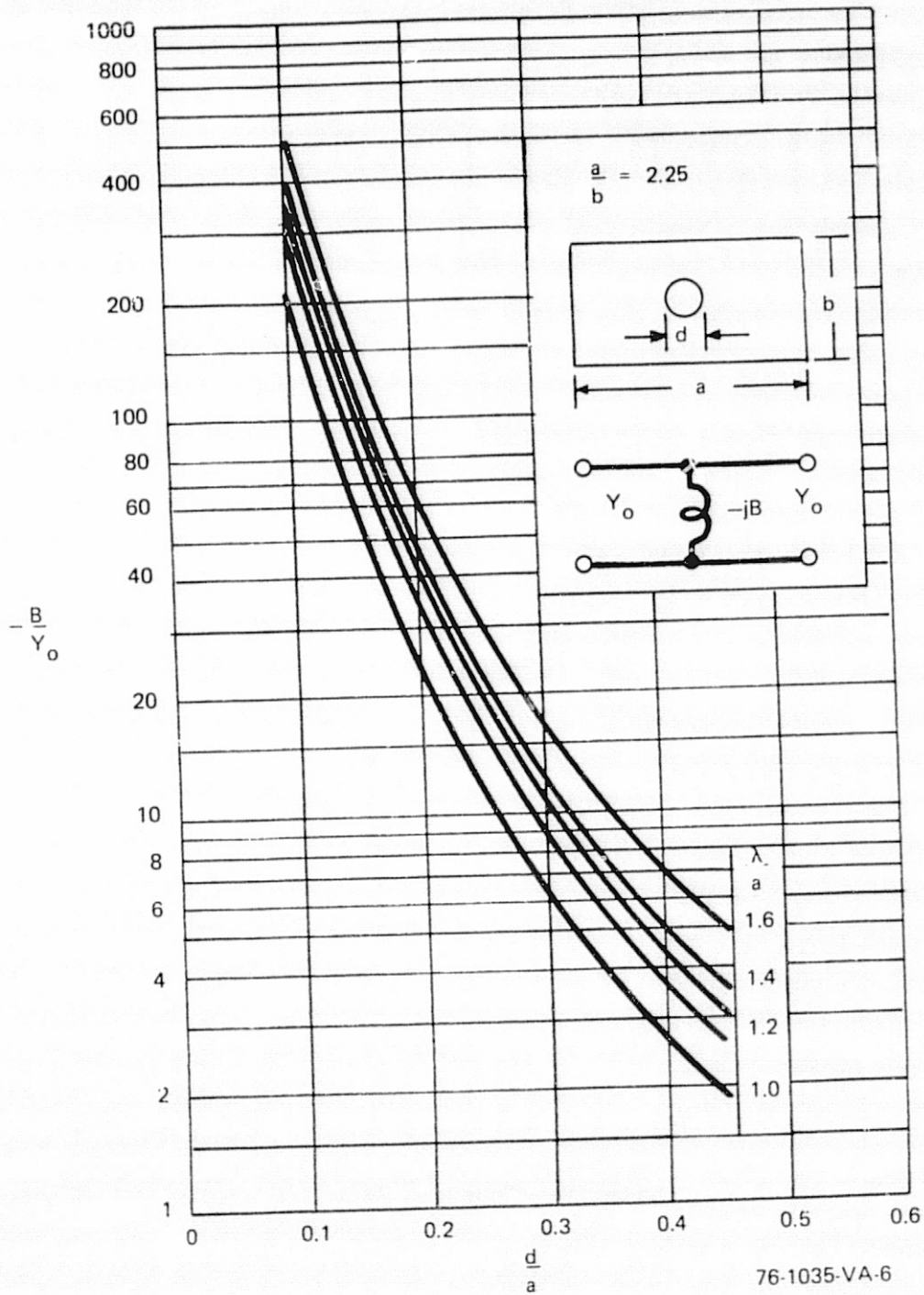


Figure 2-15. Susceptance of Thin Iris in Waveguide

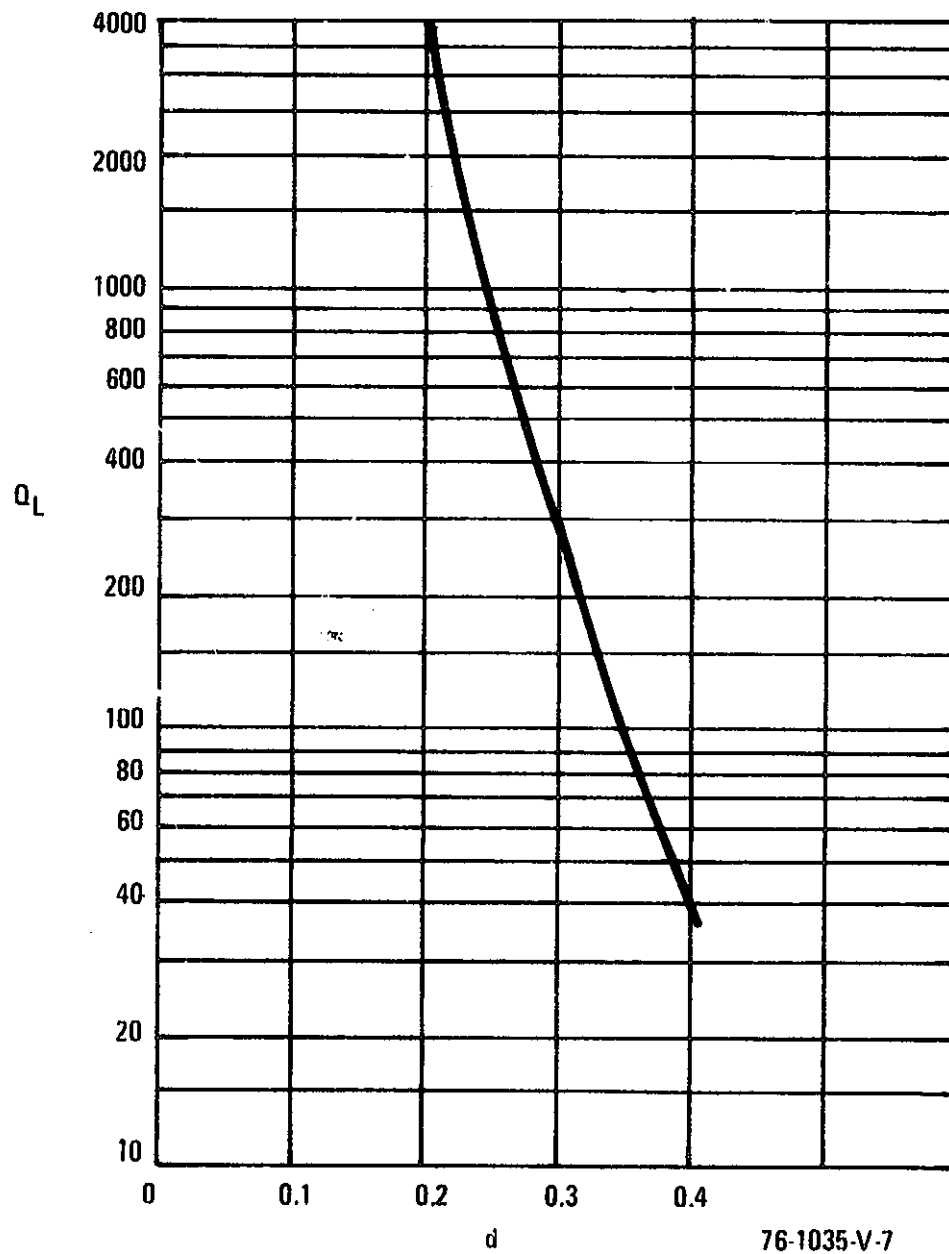


Figure 2-16. Loaded Q of Waveguide Cavity as Function of Iris Diameter d

The compensation is obtained by critical adjustment of the tuning rate and shaft length. The higher the tuning rate the shorter can be the shaft length for a given amount of compensation. The highest tuning rate is achieved with a high dielectric constant tuner material called Lucalox. Quartz could have been used as the tuner but a longer shaft would have been required to achieve the same degree of compensation.

2.1.4 Converter Performance

The complete converter comprises the image enhanced mixer and the local oscillator. Figure 2-17 is a photograph of the final unit. The MIC mixer is mounted in a machined housing which contains the SMA connectors for RF insertion and IF and Beacon signal removal. Also contained in this housing is a printed circuit board holding the bias voltage regulator for the Gunn oscillator. Figure 2-18 is the schematic diagram for the Gunn diode voltage regulator.

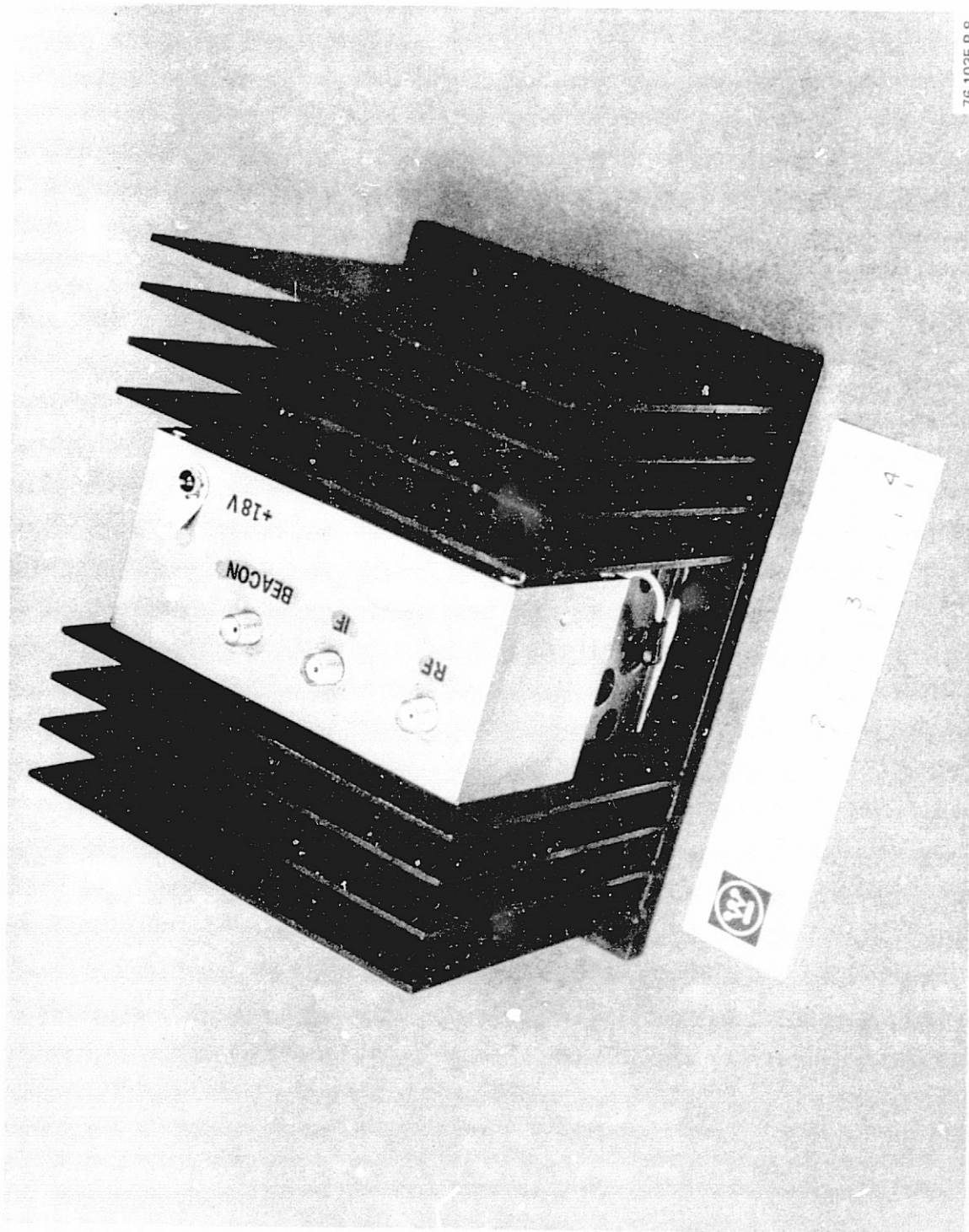
The LO and mixer assembly is affixed to a finned heat sink. Thermal considerations for the oscillator dictate a temperature differential (oscillator body temperature to ambient temperature) of 15°C to maintain the diode junction at a safe reliable temperature. As convective cooling is being used, then about 125 square inches of surface is required, thus the eight fins of nominally 2 x 4 inch dimension. If conductive cooling is possible; i.e., if a low thermal impedance path is assured by the mounting arrangement, then the fins could be reduced in size or even eliminated.

The final performance data for the three delivered converters is presented in Table 2-1.

2.2 PARAMETRIC AMPLIFIER

This program to develop a 12 GHz paramp was run concurrent with a very similar program to develop a 9.3 GHz paramp. Many of the theoretical

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Figure 2-17. Complete Converter

TABLE 2-1: CONVERTER PERFORMANCE DATA

| | | | |
|---|------------------------|-----------------------|-----------------------|
| f_{RF} (GHz) | 12.0 - 12.15 | | |
| f_{LO} (GHz) | 9.4858 | | |
| | Unit #1 | #2 | #3 |
| RF Return Loss (dB) | 13 | 19 | 13 |
| IF Return Loss (dB) | 15 | 16 | 10 |
| Conversion Loss (dB) | | | |
| at 12.00 GHz | 3.80 | 3.60 | 3.40 |
| 12.05 | 3.60 | 3.60 | 3.60 |
| 12.10 | 3.62 | 3.70 | 3.80 |
| 12.15 | 3.90 | 3.75 | 3.75 |
| Beacon 11.7 | 7.52 | 8.5 | 8.1 |
| Noise Ratio (N.R.) | 1.6 | 1.0 | 1.25 |
| $F_{MIX} = L_C (F_{IF} + N.R. - 1) (F_{IF} = 6.4 \text{ dB}, f_{RF} = 12.05)$ | | | |
| at Temp. -50°C | - | 9.65 | 10.33 |
| -25°C | - | 9.90 | 10.38 |
| 0 | - | 10.01 | 10.36 |
| 25 | - | 10.12 | 10.33 |
| 50 | - | 10.27 | 10.34 |
| LO Stability (-50°C to +50°C) | $\pm 0.75 \text{ MHz}$ | $\pm 1.3 \text{ MHz}$ | $\pm 1.0 \text{ MHz}$ |
| 3rd Order Intermod Products with signals at -55 dBm (dB below IF) | - | 137 | 138 |

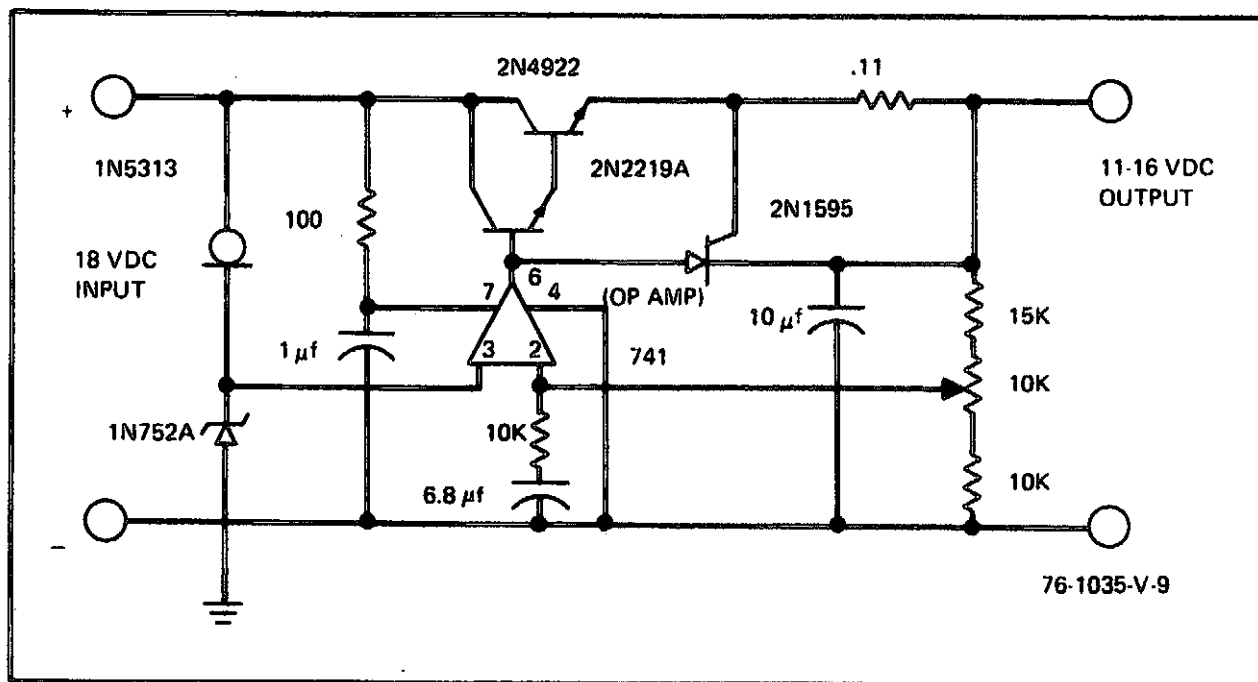


Figure 2-18. Gunn Diode Voltage Regulator

developments and actual components described in this report were common to the two programs. Because of the great difficulties encountered, the only actual recorded paramp performance was at 9.3 GHz. The problem areas which severely limited the scope of the results were the idler and pump transmission circuits which were common to both programs. The following sections of the report reflect the commonality of technology and component development.

Figure 2-19 is a plan view of the paramp initial design. The outer dimensions of the layout shown are 2.5 inches by 3.25 inches. The 5 - port signal ferrite circulator has been incorporated to ensure satisfaction of the VSWR, gain, and phase stability requirements. There are four IC substrates identified in Figure 2-19. Substrate -1 (S-1) comprises the complete 5 - port signal circulator. Substrate - 2 (S-2) contains microstrip for signal

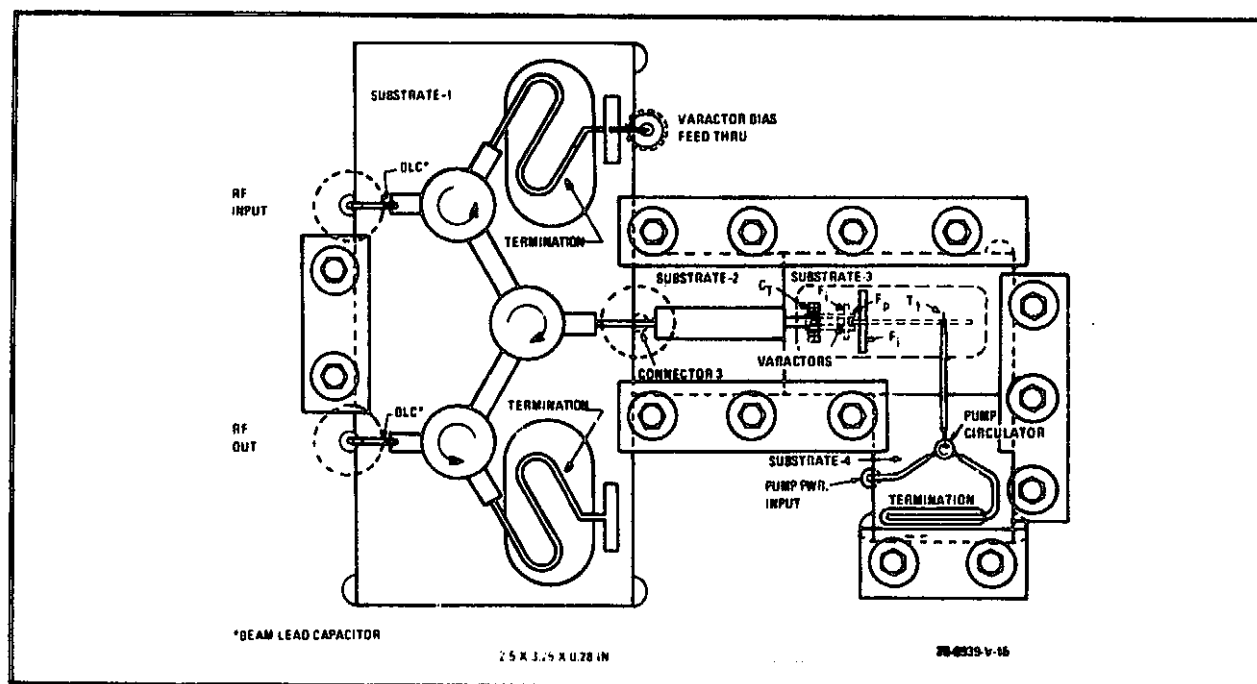
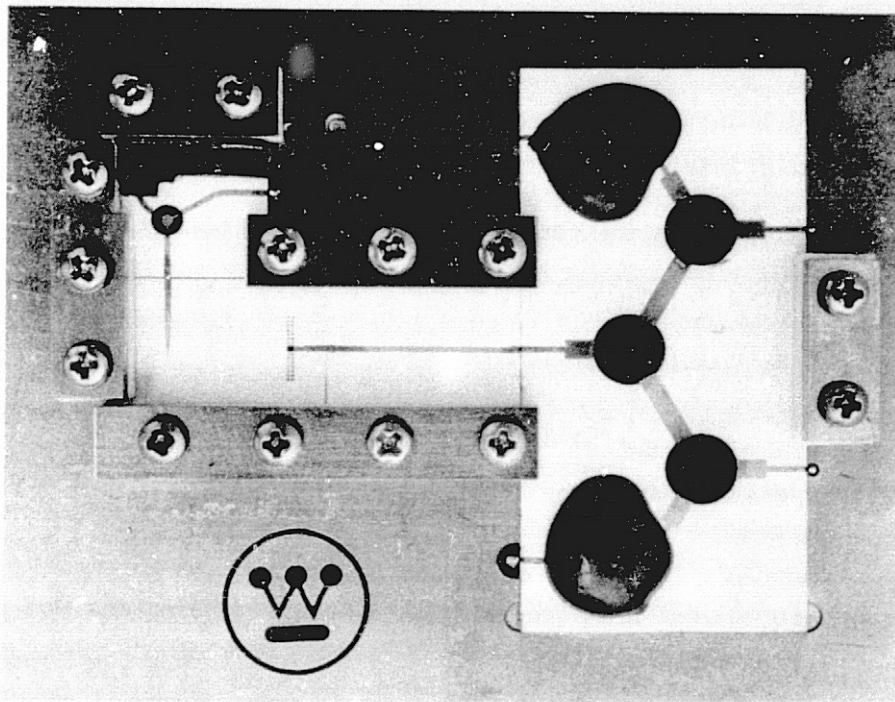
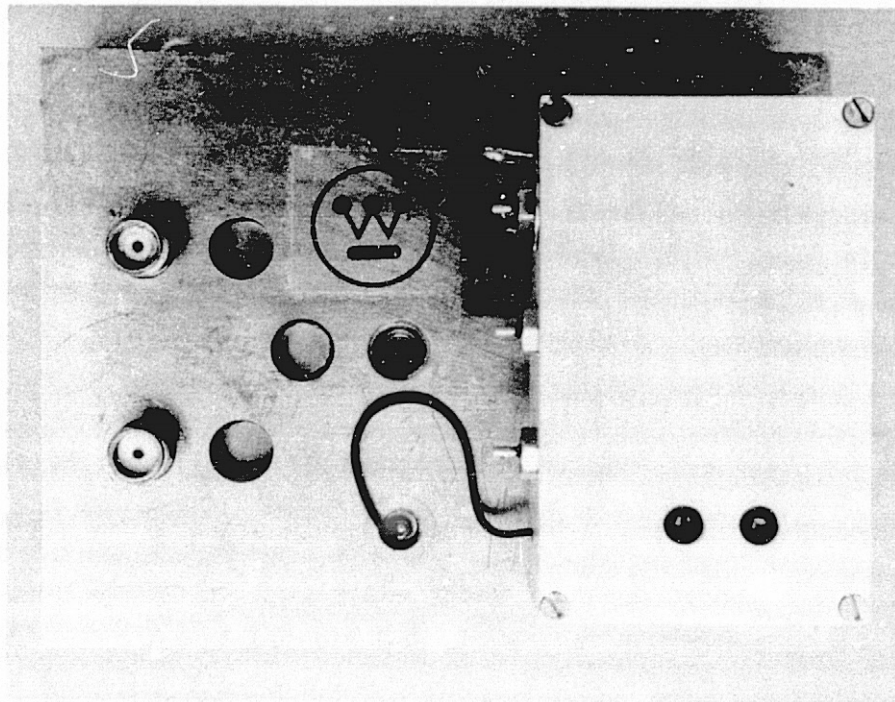


Figure 2-19. X-Band Paramp Layout

impedance matching to the varactors. Substrate -3 (S-3) contains a coplanar line-slot line junction and the special varactor chip developed for this application. The chip contains a pair of high f_{co} GaAs Schottky barrier varactors so arranged as to facilitate bonding to the coplanar line-slot line junction. S-3 also contains the microstrip to coplanar line transition with the initial capacitive elements, C_T , for tuning the varactors to the center signal frequency. Also on S-3 are the slot line idler and pump isolation filters, F_i and F_p , and the transition to microstrip from slot line for the pump injection. Substrate -4 (S-4) contains the pump ferrite isolator (terminated circulator) and the waveguide to microstrip coupling means for pump power coupling from the ADO cavity which is located immediately below and adjacent to S-4.

Figure 2-20 is a photograph of the assembled initial design.

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Figure 2-20. Initial Paramp

Figure 2-21 and 2-22 are photographs of the final amplifier. Substrate -3 has been modified and substrate -4 (pump isolator) has been eliminated. The pump cavity has been removed by use of a waveguide coupling element.

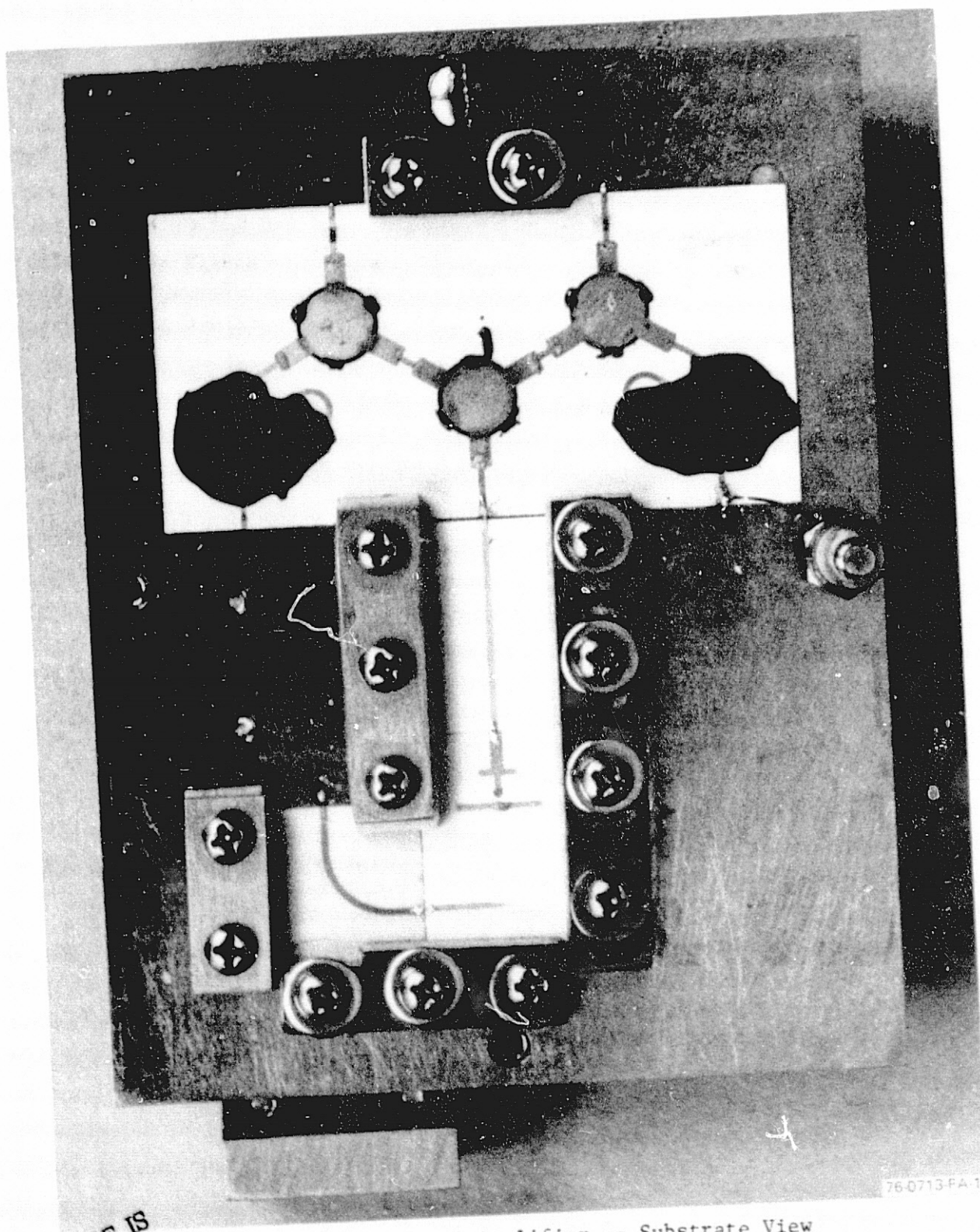
The measured results obtained with the unit pictured in Figures 2-21 and 2-22 are given in Table 2-2.

2.2.1 Paramp Components

As was noted in the preceding discussion, the components developed for the integrated parametric amplifiers include a 5 - port ferrite signal circulator, a broadband low loss microstrip to coplanar waveguide transition, a low loss and well balanced coplanar waveguide-slot line hybrid junction, a special varactor chip containing a pair of matched high f_{co} GaAs Schottky barrier varactors, a slot line and microstrip idler rejection filter and pump matching circuit, a broadband low loss transition between microstrip and slot line for the pump circuit, a pump ferrite isolator (terminated microstrip circulator), and a special high Q ADO circuit with efficient means for coupling to microstrip without destroying the high Q of the oscillator circuit. Also there is a Varactor Bias Regulator and Pump Leveler Circuit.

2.2.1.1 Microstrip Signal Circulator

A component of primary concern in the development of any low noise negative resistance amplifier is the wide band input signal circulator. A photograph of the first 3 - port is shown in Figure 2-23. The isolation was greater than 20 dB for 1.0 GHz of bandwidth. The insertion loss was under 0.5 dB for about 700 MHz of bandwidth. The 5 - port version (as seen in Figure 2-21) was based upon a modified version of that shown in Figure 2-23. The insertion loss for the 5 - port was about 0.6 dB over 1.0 GHz of bandwidth. The isolation was greater than 30 dB over 1.0 GHz of bandwidth.

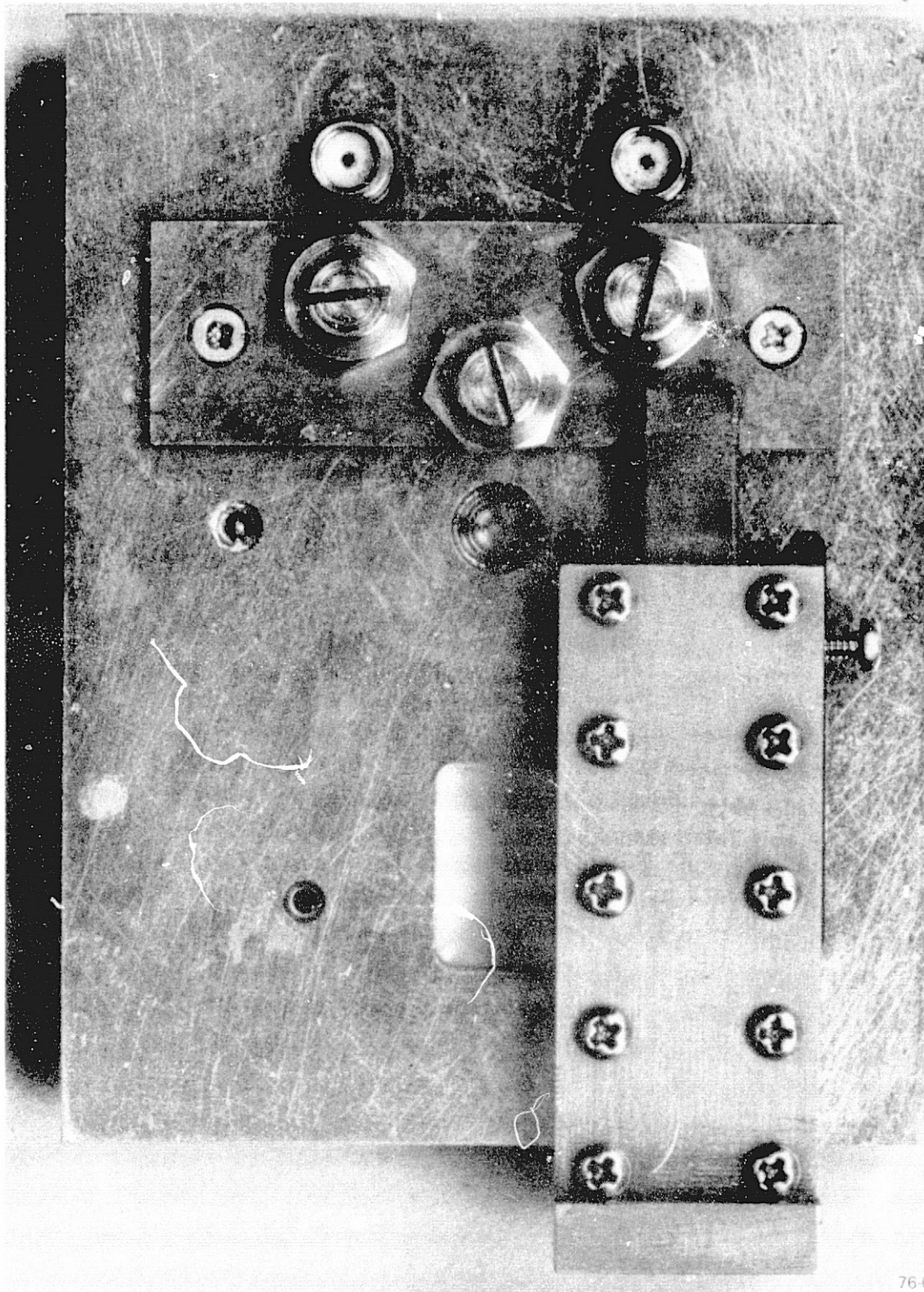


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Figure 2-21. Final Amplifier -- Substrate View

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Figure 2-22. Final Amplifier -- External View

TABLE 2-2: MEASURED PERFORMANCE - PAR/MP (Figures 2-21 and 2-22)

| | |
|------------------|----------------------------------|
| Center Frequency | 9.2 GHz |
| Pump Frequency | 35.2 GHz |
| Gain | 15 dB |
| Bandwidth | 120 MHz (single tuned bandwidth) |
| Noise Figure | 2.5 dB (2.3 - 2.8 dB) |

2.2.1.2 Pump Isolator

The pump isolator is a ferrite circulator with one port terminated. This circulator is made by embedding a ferrite disc in the alumina substrate and using both the ferrite diameter and metalization pattern to define the circulator junction. The pump frequency was initially taken to be 37 GHz. The performance data on this device is given in Figure 2-24. The performance of this unit was acceptable for the pump isolator as the only task for this isolator is to improve the stability of the pump oscillator. However, the isolation band was centered about 3 GHz low and was to be increased. This increase was designed into the second isolator which is shown mounted in Figure 2-20. However, all performance data was not taken on this second model. A close-up photograph of the second unit is shown in Figure 2-25.

The use of this isolator was subsequently abandoned as the losses of the slot line and microstrip coupling line appeared to be sufficient to allow stability of the pump oscillator.

2.2.1.3 Pump Oscillator - IMPATT Design

Figure 2-26 shows a photograph of the implemented version of the pump oscillator, but with the pump oscillator coupled to a waveguide for test purposes. The coupling means initially took the form of a slot line aperture

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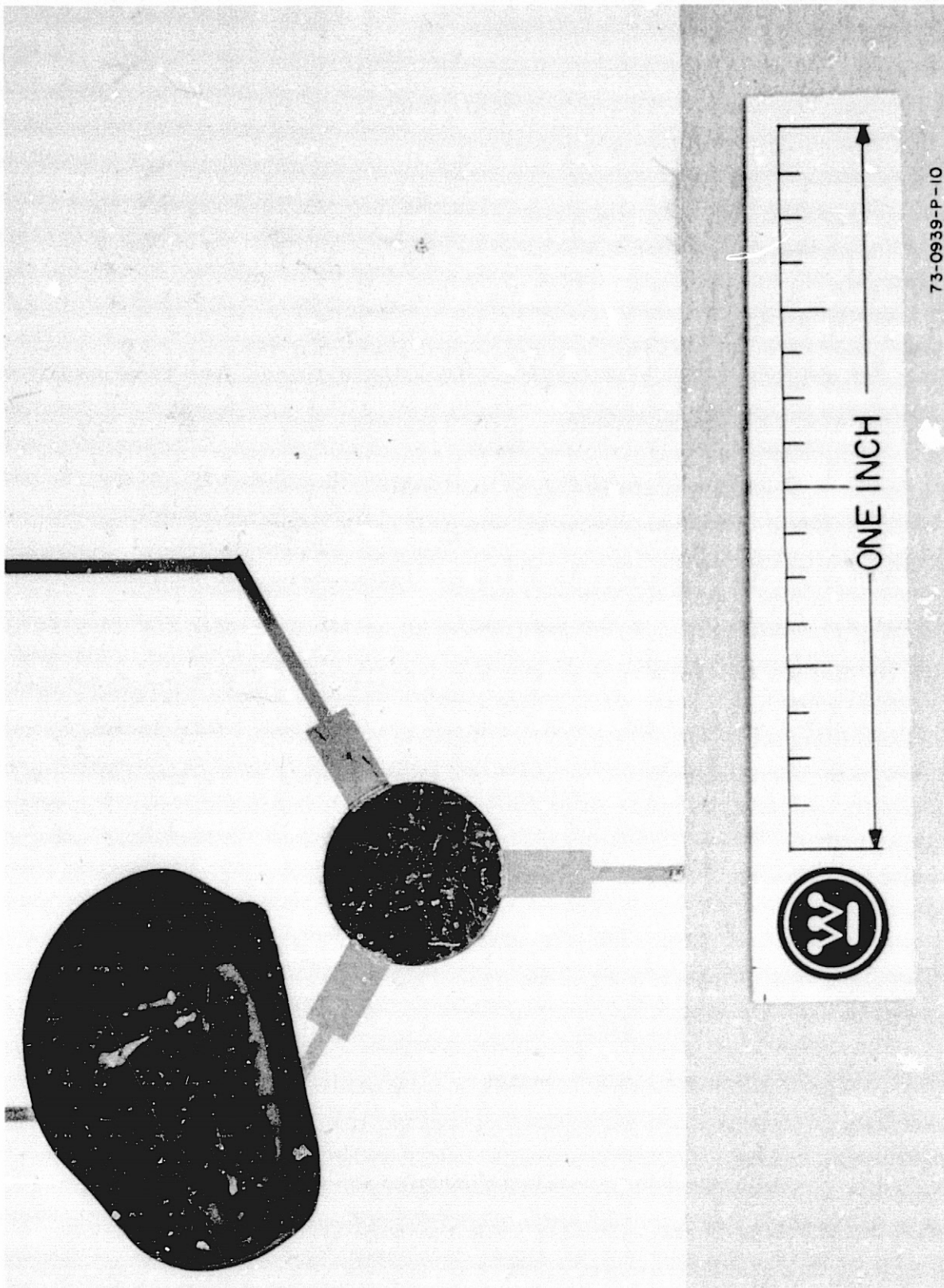


Figure 2-23, 3-Port Signal Circulator

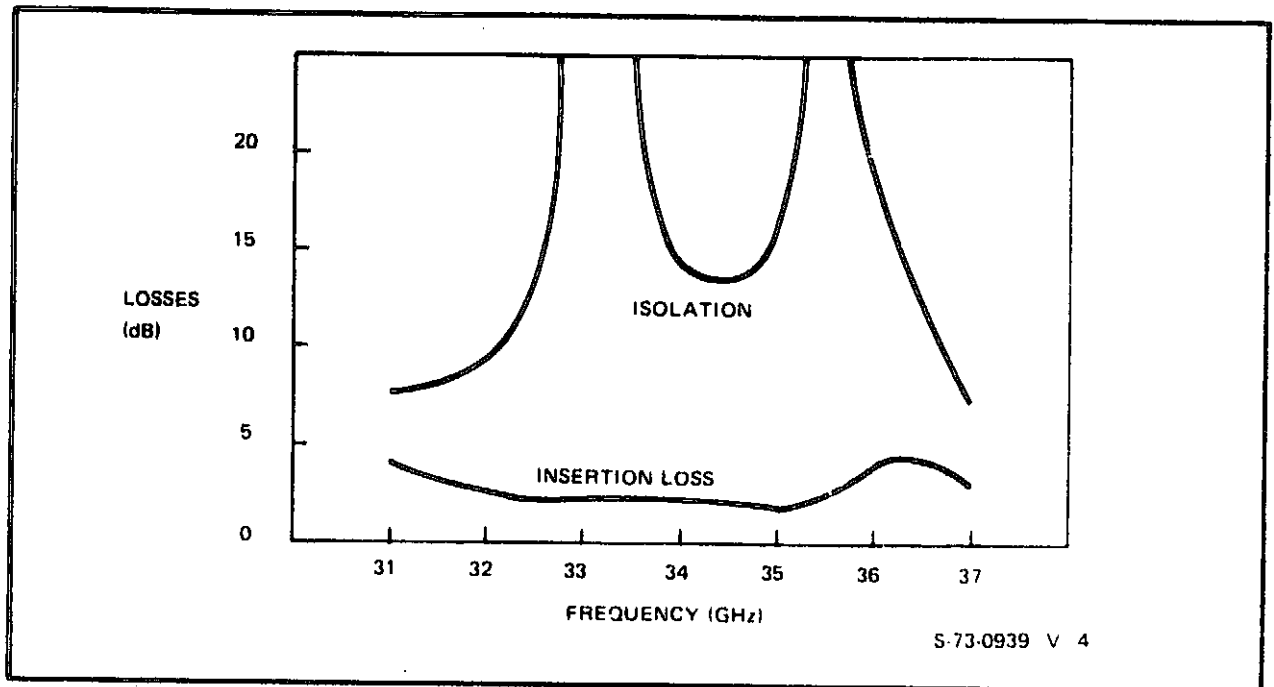


Figure 2-24. Performance Data -- Pump Isolator

coupling to microstrip. That was changed to a probe coupling from the cavity to microstrip. This form then allows equal facility for coupling from the cavity to waveguide for test purposes.

It is shown in a later section that nominally 10 mW of pump power in the paramp diodes was required. The oscillator shown in Figure 2-26 has supplied in excess of 80 mW and with slightly higher drive in the ADO, pump power of 100 mW is available. The oscillator is capable (with different cavities) of oscillating over a frequency range of 26 - 40 GHz with the same diode.

Figure 2-27 is a photograph of the interior of the ADO pump source, showing the cavity, diode with top-hat resonator, and the fine wire bias lead terminating in the stabilizing resistance material.

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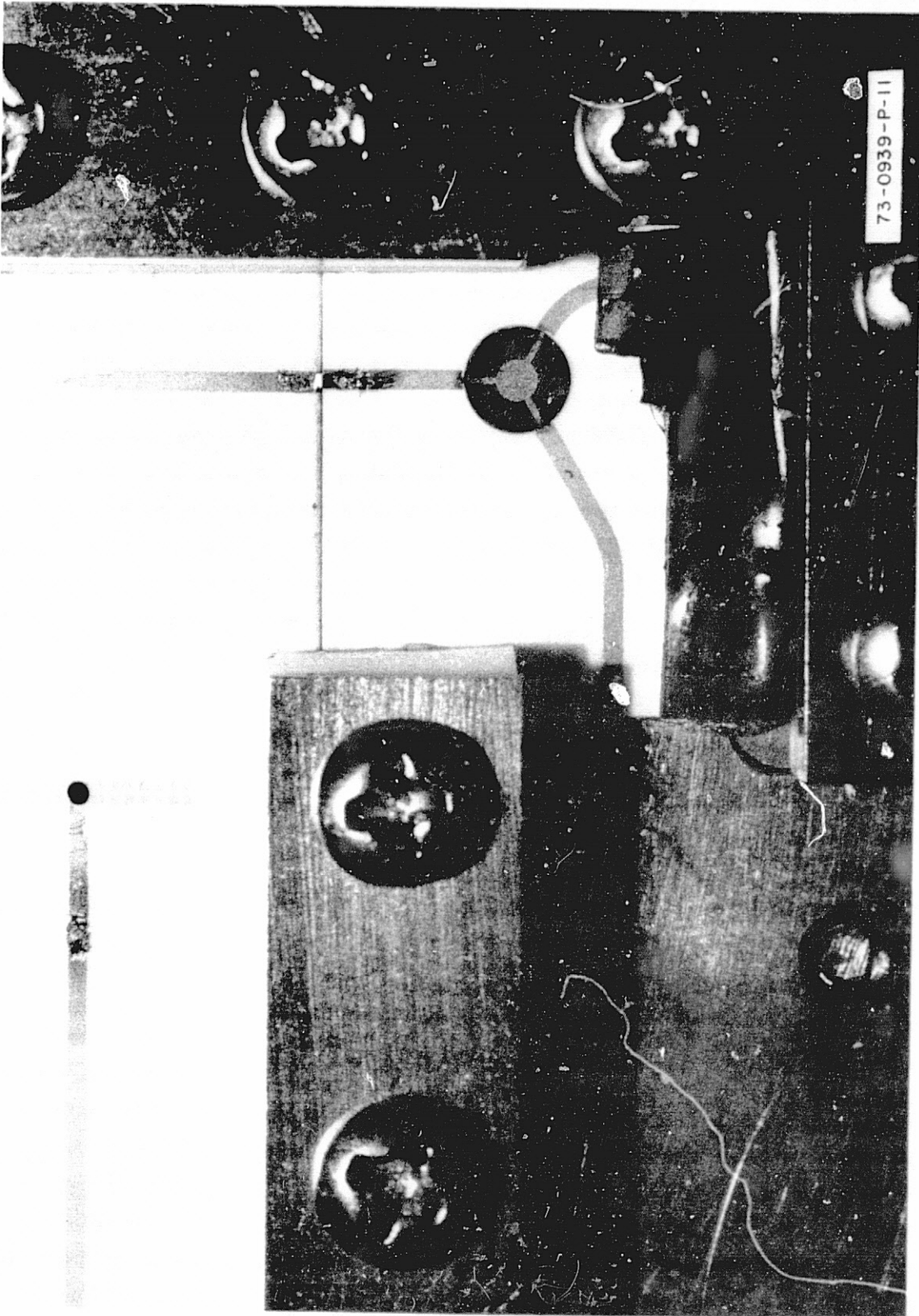
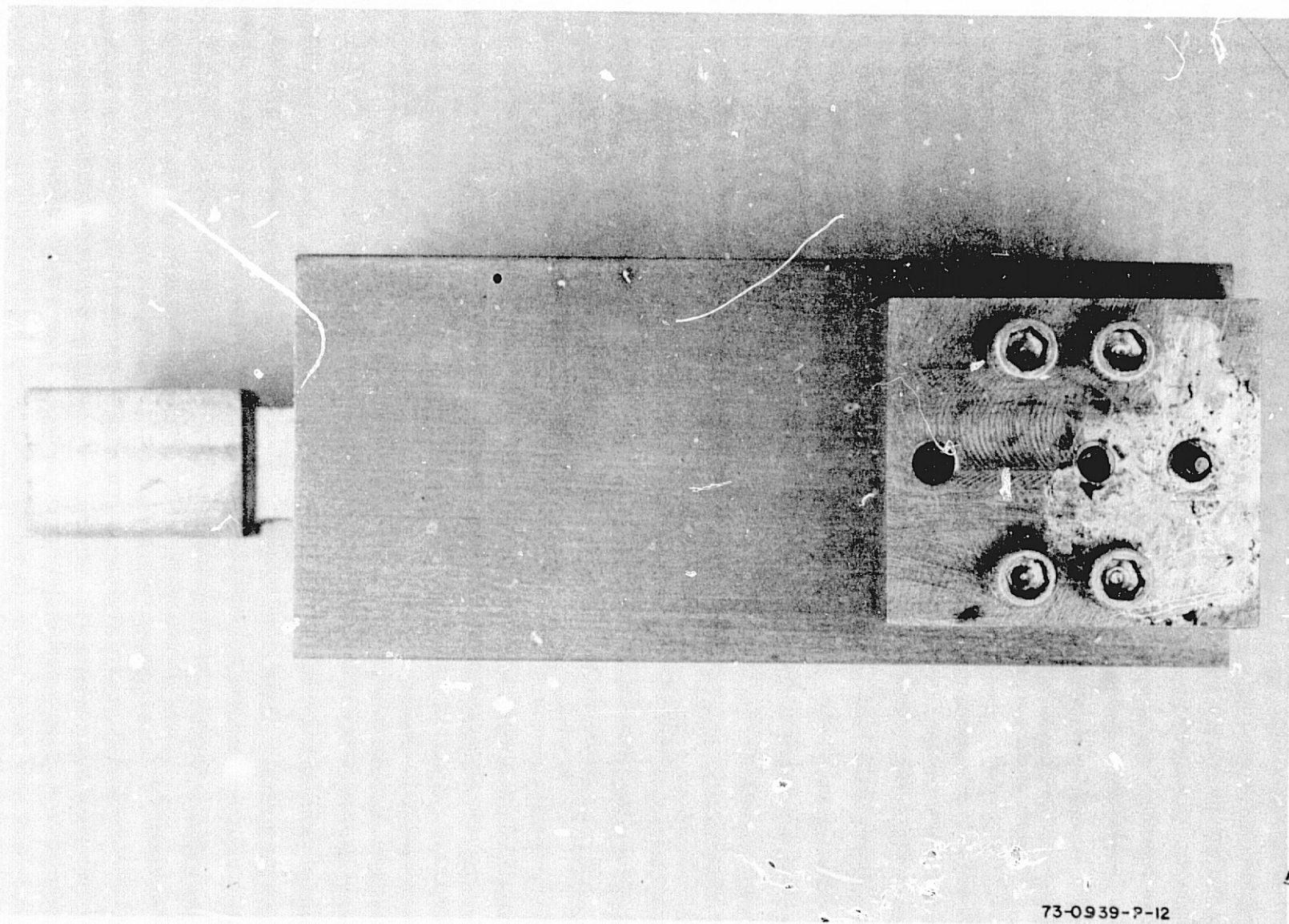


Figure 2-25. Pump Isolator

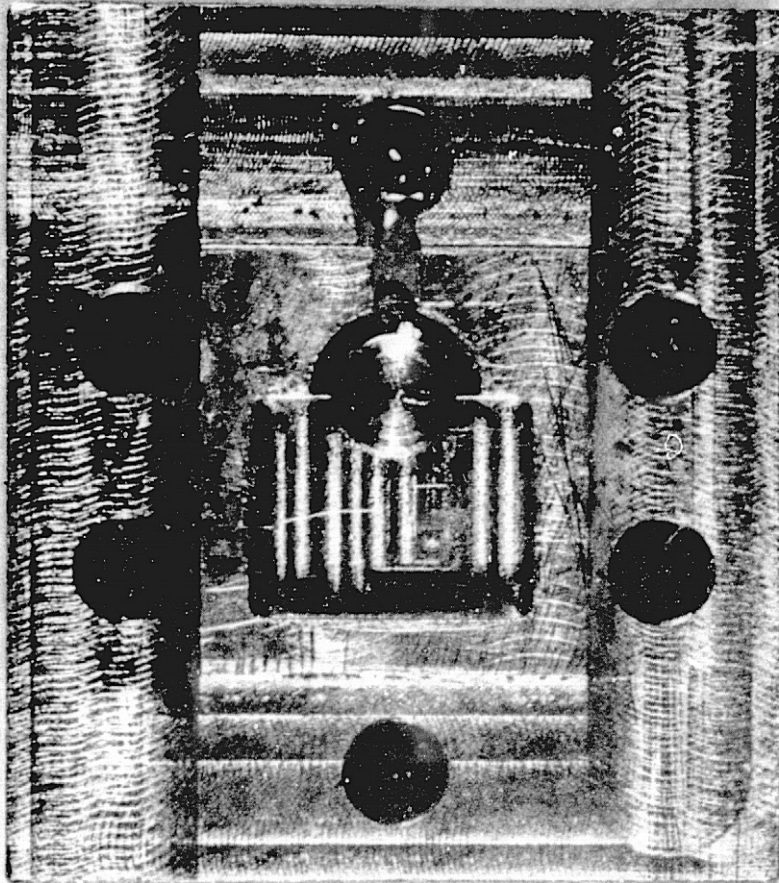


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Figure 2-26, Pump Oscillator (ADO) Coupled to Waveguide

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Figure 2-27. Interior of ADO Pump Source

Figure 2-28 is a set of curves showing oscillator performance at a given ambient temperature and given output power and frequency, as a function of dc input current. These parameters are critical to the paramp performance as they will determine just how well the oscillator will work in conjunction with the pump leveler circuit. The curve of RF power versus dc power must be smooth and monotonic with no hysteresis.

The oscillator pictured has delivered up to 80 mW at 37 GHz using a commercially available silicon IMPATT diode. In varying the dc input power to cause the oscillator to go from threshold to maximum power output, a frequency deviation of on the order of 100 MHz encountered. This indicates that the stabilizing cavity appears to be operating as desired.

2.2.1.4 Pump Oscillator - Gunn Design

In the amplifier shown in Figures 2-21 and 2-22, a Gunn Diode pump oscillator was actually used. The Gunn oscillator cavity and diode mounting structure was more easily fabricated and reproduced than the IMPATT unit and the resulting oscillation was more stable and spurious free than the IMPATT. An external constant voltage source was used to power these oscillators. The regulator circuit to be described in paragraph 2.2.2.7 could not be used with this oscillator because it was designed to give a controlled constant current output (high source impedance) as required by the IMPATT rather than the controlled constant voltage (low source impedance) as required by the Gunn devices.

The design approach taken with this Gunn device is shown in Figure 2-29. This is about the least complex, most cost effective design that could be implemented for a demountable waveguide oscillator. The oscillator comprises a simple machined housing (could be cast aluminum for cost effectiveness) and four machined parts (which in a later design has been reduced to two),

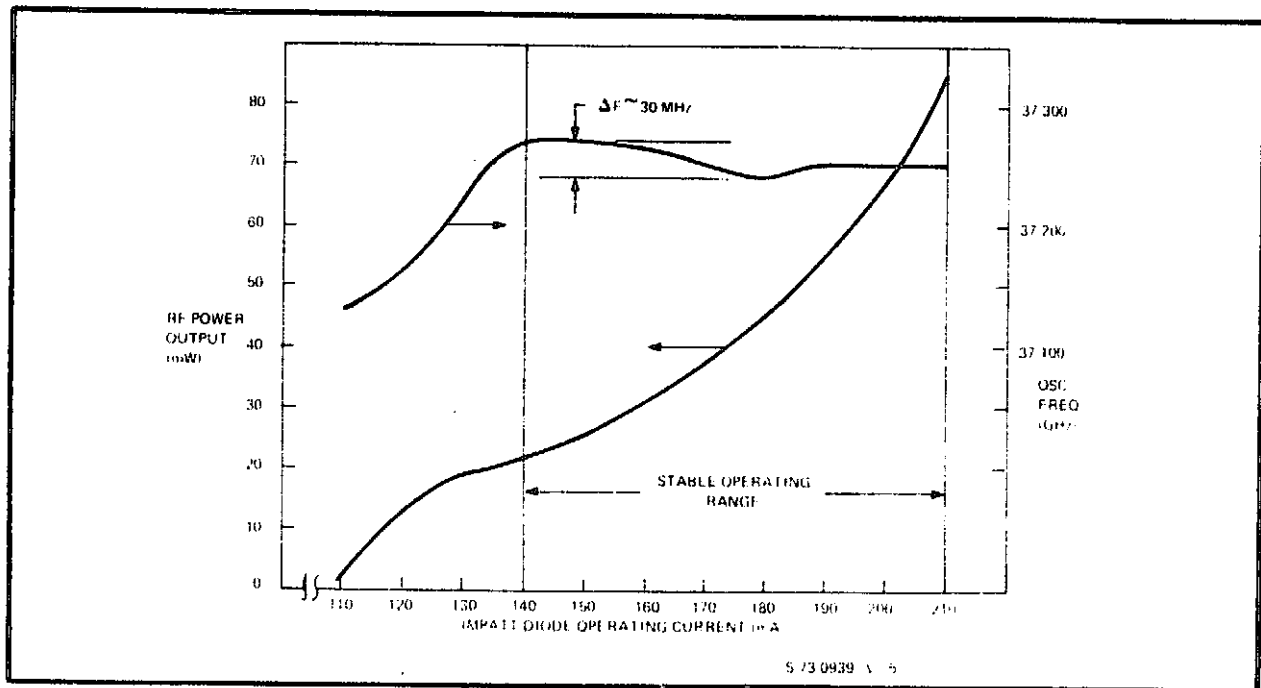


Figure 2-28. Pump Oscillator (ADO) Performance Curves

A Johanson dielectric tuner (#6933) is used for mechanical frequency adjustment. The diameter of the radial line resonator determines the fundamental oscillator frequency; the use of the dielectric tuner allows nominally a 3-4 GHz tuning range with negligible variation in oscillator output power. The output power for these oscillators range from 80-130 mW.

For a given diode (of a specific impedance level) the center frequency and power output (impedance matching to the waveguide) are adjusted by varying the diameter of the radial line resonator and the diameter (D) of the connecting post. The resonator is made up of two parts: the space below the radial line resonator in which is embedded the Gunn device, and the space above the radial line resonator to the connecting post. The basic resonant frequency is determined by the total path length around the radial line

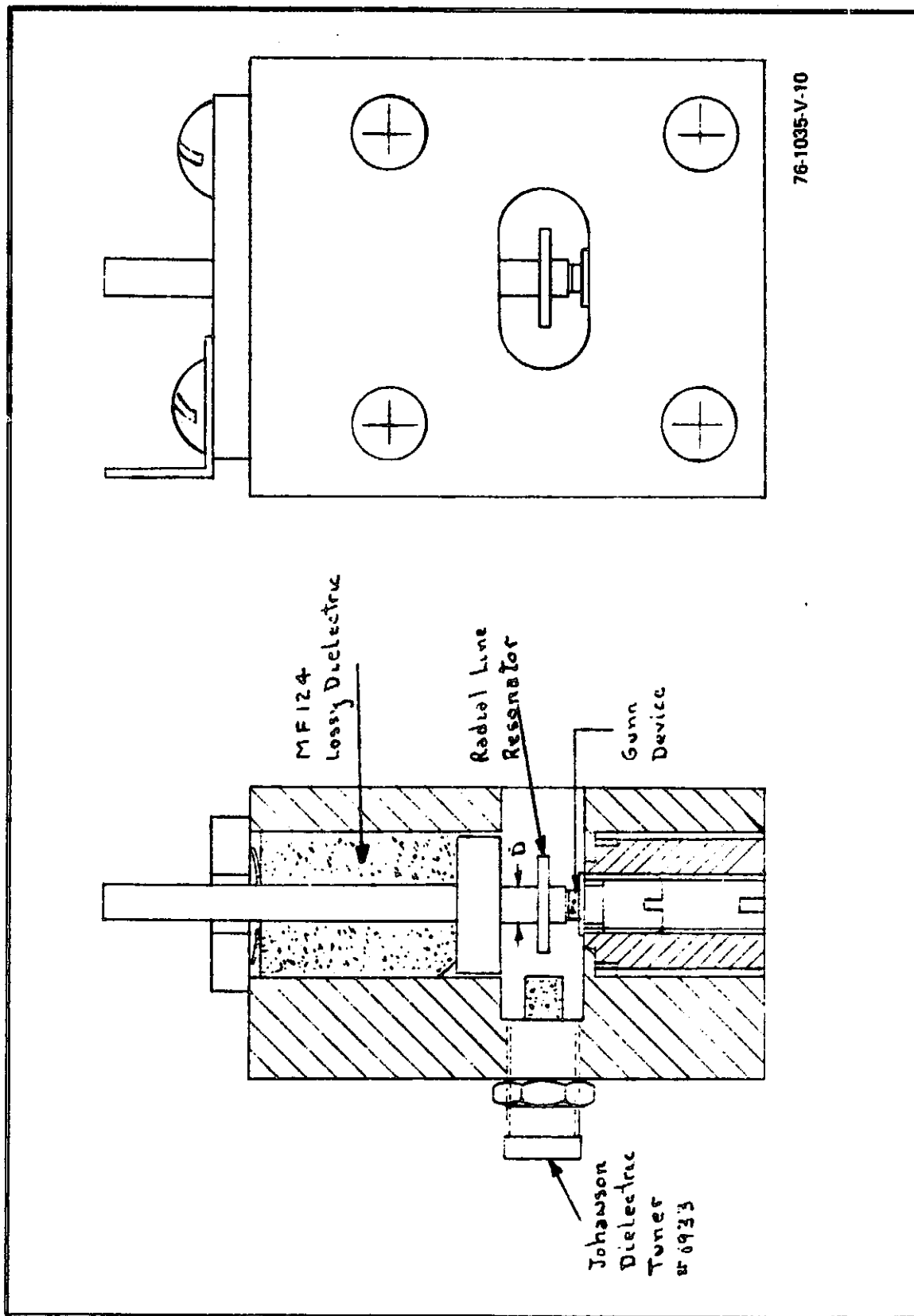


Figure 2-29. 37-GHz Pump Oscillator -- Gunn Design

resonator from the active (Gunn) device to the periphery of the center (connecting) post. The coupling to the waveguide is determined by the unbalance in the local fields above and below the radial line resonator.

2.2.2 Paramp Design

Several factors influence the selection of the varactor and the number of gain stages to be used for a particular amplifier design. These include (1) the dynamic quality factor (\tilde{Q}) at the signal and idler frequencies (for minimum noise figure, Q should be as high as possible), (2) ease with which the varactor diode can be resonated to the idler frequency, (3) the capacitance modulation factor (γ), which must be as large as possible to obtain maximum bandwidth, (4) the varactor must be capable of being pumped hard enough to ensure compatibility with the operational requirements of signal saturation (gain compression), and (5) the varactor should not require such large amounts of pump power that a solid-state pump source cannot be used.

2.2.2.1 Amplifier Noise Figure

Before the pump power level, signal saturation, etc., can be determined, the pump frequency must be specified. The pump frequency is determined by the noise figure requirement and the limitations this places on the idler frequency. It is desirable to maintain the idler frequency (f_i) as low as is possible.

Thus, we first proceed to calculate the overall theoretical noise figure (noise temperature) of the amplifier. The noise (loss) contributing elements in the signal input circuit, with their assumed losses are given in Table 2-3.

TABLE 2-3
AMPLIFIER SIGNAL CIRCUIT LOSSES

| <u>Component</u> | <u>Losses (dB)</u> |
|--------------------------------------|--------------------|
| Input Coaxial Connector | 0.10 |
| Circulator Junctions (2 each) | 0.20 |
| Double Tuning and Matching Circuitry | <u>0.20</u> |
| Total Input Losses | 0.50 |

The input and output circuits are essentially identical so the same losses apply to the two circuits. Figure 2-30 is a sketch showing the assumed amplifier configuration and indicated losses.

The diode noise temperature, T_{eq} , is obtained through evaluation of equations¹² 2-6 to 2-8, or reference to Figure 2-31.

$$T_N = T_O \left(\frac{f_s}{f_i} \right) \left[\frac{\tilde{Q}_{es}^2 + \left(\frac{f_i}{f_s} \right)^2}{\tilde{Q}_{es}^2 - \left(\frac{f_i}{f_s} \right)^2} \right] \quad (2-6)$$

$$= T_{eq} \left(\frac{T_O}{T_d} \right) \quad (2-7)$$

where

T_{eq} = equivalent (excess) noise temperature of the varactor diode and mount

$T_O = 290^\circ \text{ K}$

T_d = diode junction temperature ($^\circ\text{K}$)

$\tilde{Q}_{es}^2 = \frac{\gamma^2 (f_{cs} \cdot f_{ci})}{f_s^2} = (\text{effective signal dynamic } Q)$

and f_{cs} , f_{ci} are the cutoff frequencies measured at the signal and idler frequencies, f_s and f_i respectively.

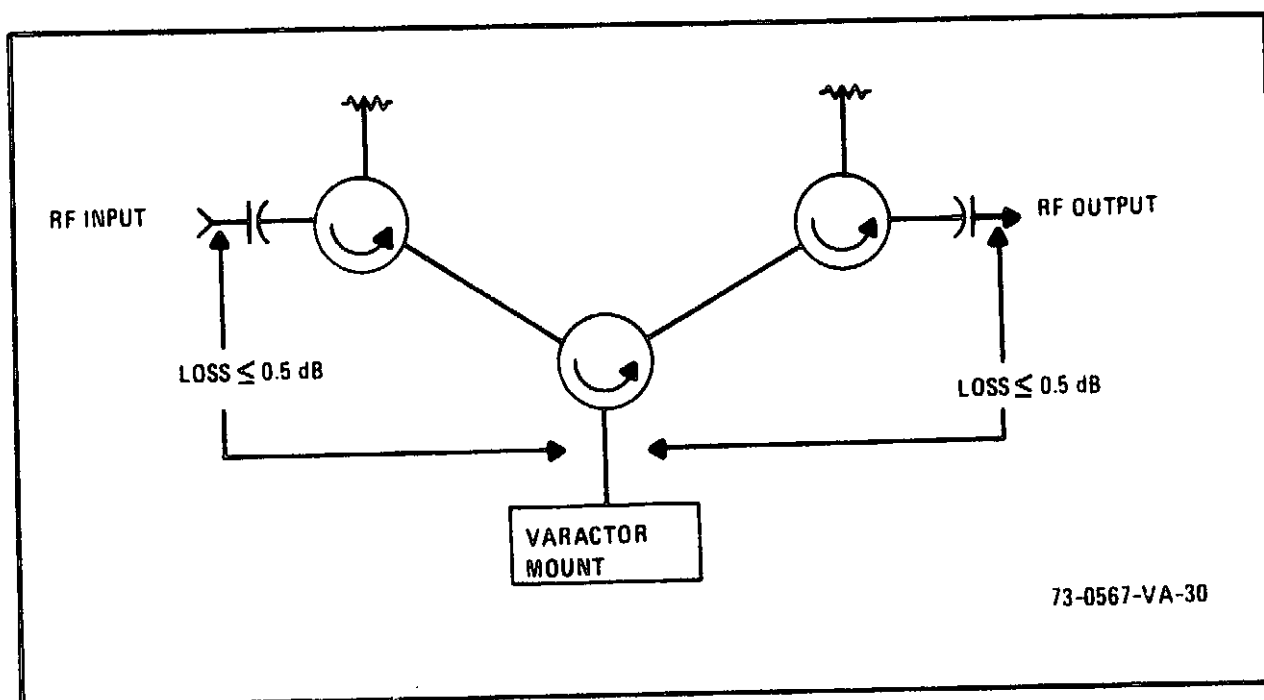


Figure 2-30. Parametric Amplifier Configuration Showing Signal Circuit Losses

The GaAs Schottky barrier junctions regularly made at Westinghouse now have a cutoff frequency greater to or equal to 800 GHz at zero bias. Thus, assume $f_{ci} = 800$ GHz at zero bias (f_{ci} goes $\approx 1,000$ GHz at V (bias) ≈ 0.6 volts). Essentially, 800 GHz is that value measured at 70 GHz in the reflectometer setup. Assuming a 2:1 degradation in cutoff frequency on the signal side, $f_{cs} = 500$ GHz. Thus $\tilde{Q}_{es} = 12$ if the capacitance modulation coefficient, γ , is taken to be $\gamma = 0.2$. The value $\gamma = 0.2$ is a very low value, but one which is realistic in view of the junction overlay used in the diode fabrication process.

As the goal for the overall amplifier gain was 15 dB, and the input and output losses total 1.0 dB, the actual varactor gain must be 16 dB. It is desired to obtain an overall amplifier noise figure of less than 2.5 dB. This

would require the paramp (less the input signal circuit loss) noise figure to be less than 2.0 dB, or T_{eq} less than 170°K. Using equation 2-7, and taking the diode junction temperature to be about 325°K, the required value of T_N is 152°K. Reference to Figure 2-31 shows that an idler to signal frequency ratio of 2 will be satisfactory; i.e., $f_i = 24$ GHz and $f_p = 36$ GHz.

Thus the parameters become: $f_s \approx 12$ GHz, $f_i = 24$ GHz, $f_p \approx 36$ GHz, $T_d = 325^\circ\text{K}$, $\tilde{Q}_{es} = 12$, and $T_{eq} = 169^\circ\text{K}$.

The cascade noise equation¹³ is used to determine the combined effects of each of the noise sources. The equation is

$$T_A = (L_1 - 1) T_1 + L_1 T_{eq} + \frac{L_1}{G} (L_2 - 1) T_2 \quad (2-9)$$

where T_A is the equivalent noise temperature of the overall amplifier; L_1 and T_1 , L_2 and T_2 are the losses through the input and output ($L_1 = L_2 = 0.5$ dB) at temperature $T_1 = T_2 = 290^\circ\text{K}$. Evaluating equation 2-9, one obtains $T_A = 225^\circ\text{K}$ for an amplifier noise figure $F_A = 2.48$ dB. Thus the noise figure goal is realistic.

2.2.2.2 Dynamic Range (Required Pump Power)

The expression¹⁴ relating saturation (input) power P_s to the required pump power P_p is given as

$$P_s = \frac{P_p}{G^{3/2}} \left(\frac{f_s}{f_p} \right) \frac{\Delta G}{G} \quad (2-10)$$

where

G = stage gain

f_s = signal frequency

$\frac{\Delta G}{G}$ = fractional change in gain

For 0.5 dB gain compression, $(\Delta G/G) = 0.108$; for 1.0 dB compression, $(\Delta G/G) = 0.206$. If the output power at the 1.0 dB compression point is

taken to be greater than or equal to -15 dBm, P_s is greater than or equal to -32 dBm. By use of equation 2-10, the pump power (P_p) is found to be greater than 6.3 dBm; for a 6.7 dB margin use $P_p = 13$ dBm or pump power of 20 mW, for an assumed gain of 17 dB.

2.2.2.3 Varactor Parameters

The relation between actual pump power and varactor diode parameters is just¹³

$$P_p = \frac{0.5 (V_b + \phi)^2}{R_s} \left(\frac{f_p}{f_{cb}} \right)^2 \quad (2-11)$$

where

$\phi = 0.9$ volts, the diffusion potential

f_p = pump frequency = 36.0 GHz

f_{cb} = frequency cutoff referred to breakdown voltage.

Now assuming a maximum diode voltage, $V_b = 5$ volts; and $P_p = 10$ mW per diode, $R_s \cong 0.76$ ohms and C_j (0.6 volts) $\cong 0.2$ PF. The junction diameter will be about 16 microns. The overlay pad for the planar diode process will cause about 0.01 pf of shunt excess capacitance; which value will cause only slight change in the modulation coefficient which calculated to $\gamma = 0.39$, showing that the initial estimate of $\gamma = 0.2$ was conservative. The resulting varactor parameters are listed in Table 2-4.

2.2.2.4 Amplifier Gain - Bandwidth Performance - (Signal Circuit Design)

The advantages of an amplifier employing a single tuned idler circuit and double tuned signal circuit have been discussed by several authors^{15,16,17} in the open literature and the techniques for the circuits analysis have been well verified.

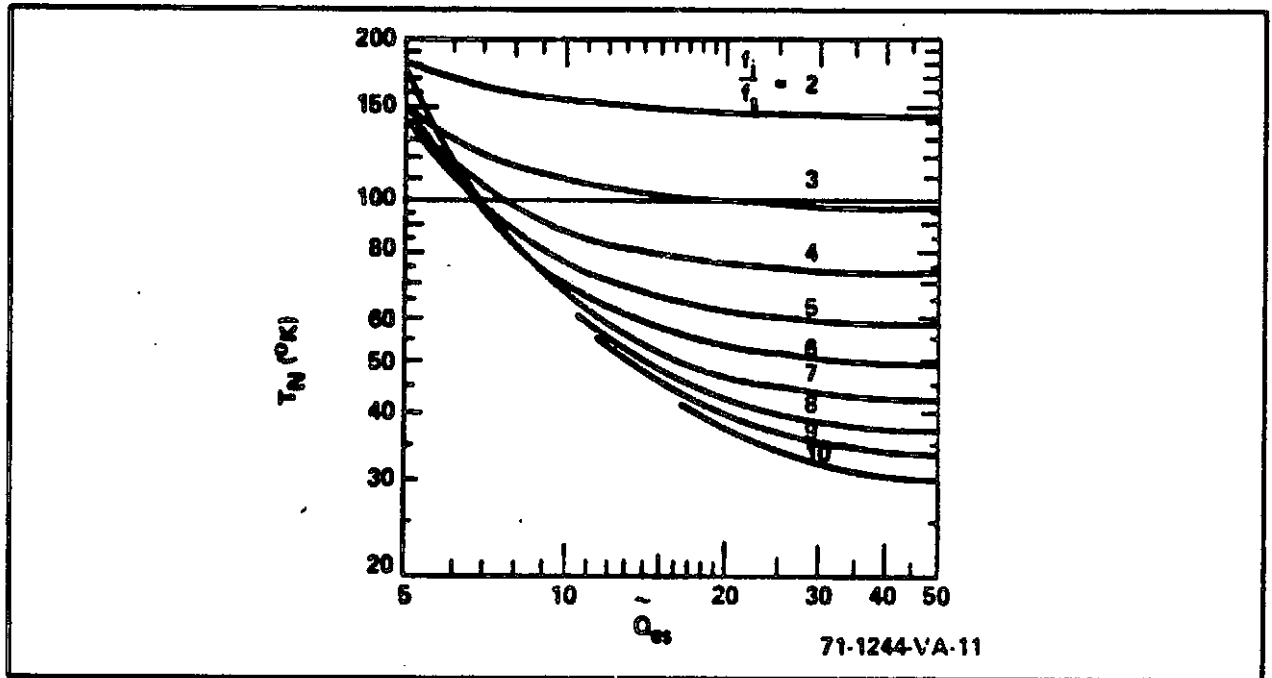


Figure 2-31. Amplifier Parameter T_N as a Function of Effective Signal Q and Idler-to-Signal Frequency Ratio

TABLE 2-4
VARACTOR DIODE PARAMETERS

| <u>Parameter</u> | <u>Value</u> |
|-----------------------------------|--------------|
| Junction Capacitance at Zero Bias | 0.26 pF |
| Series Resistance | 0.76 ohms |
| Minimum Breakdown Voltage | 5.0 volts |
| Cutoff Frequency at Zero Bias | 800 GHz |
| Pump Power per Diode | 10 mW |

Figure 2-32 shows the details of the initial varactor chip mounting and idler resonance. The idler filter, F_i , essentially open circuits the path for idler current (I_i) to the pump circuit. Thus, the idler current is confined to the simple loop shown in the circuit diagram of Figure 2-32.

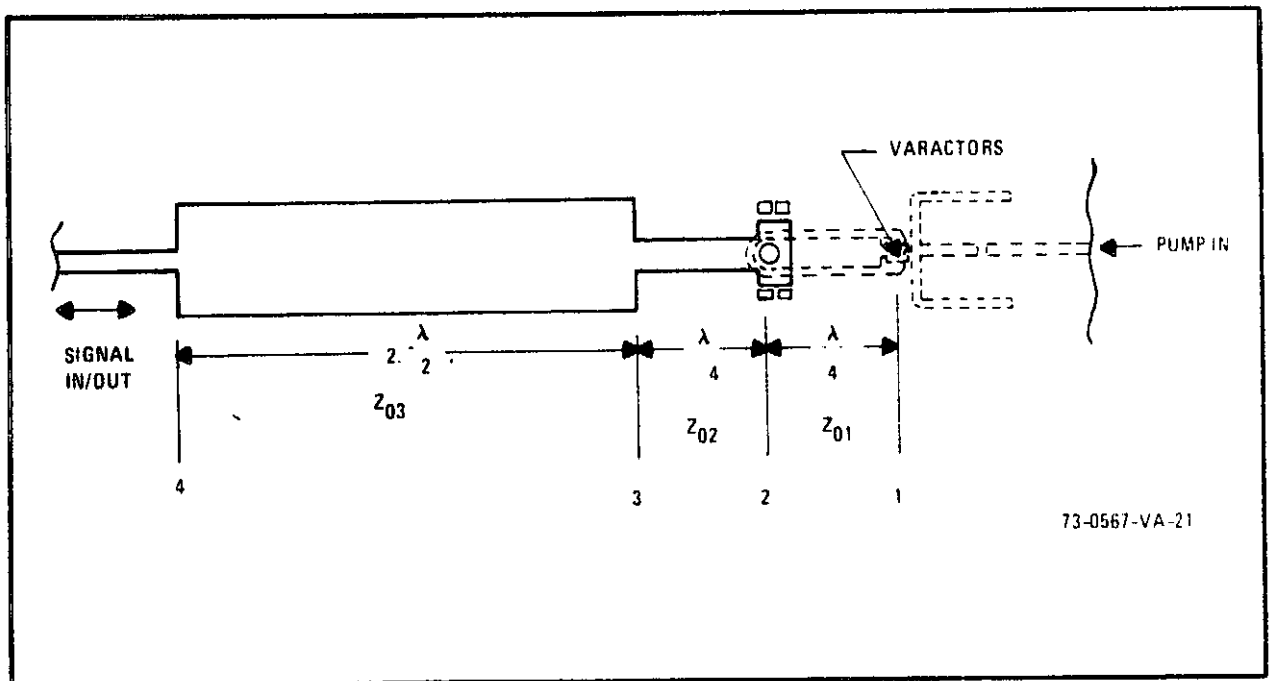


Figure 2-33. Signal Circuit Layout

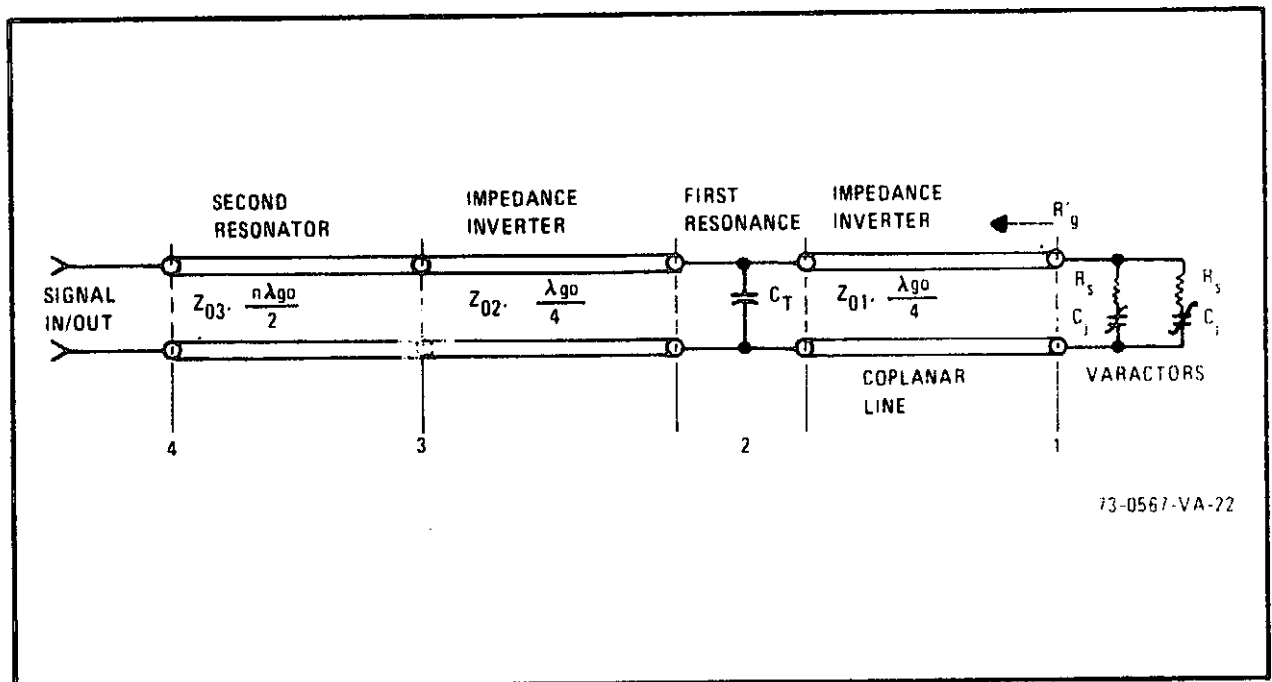


Figure 2-34. Signal Circuit -- Electrical Equivalent

$$R_{SH} = \frac{2 Z_{01}^2}{k R_s} \quad (2-12)$$

and

$$X_{SH} = \frac{2 Z_{01}^2}{X_j} \quad (2-13)$$

where R_s is given in Table 2-4, and X_j is the reactance at the signal frequency of C_j , also given in Table 2-4.

The loaded Q of the signal input network will affect the overall bandwidth of the resulting amplifier. It can be shown that the loaded Q of the first signal resonator, Q_{S1} is given by

$$Q_{S1} = \frac{X_j}{2R'_g} \left[1 + \frac{N\pi}{4} \left(\frac{2 Z_{01}}{X_j} \right) \right] = \left(\frac{X_j}{2R'_g} \right) Y \quad (2-14)$$

where N is the number (odd) of quarter wave lengths used in the coplanar line impedance inverter. R'_g is the value of the positive generator impedance at position 1 (as shown in Figure 2-34) required for the specified condition of gain and noise figure. The parameter Y shown in equation 2-14 is plotted in Figure 2-35 as a function of the ratio $X_j/2 Z_{01}$, and for $N = 1$ and 3. Note the very broad minimum in Y about the point $Z_{01} = X_j$. The parameter Y (and thus Q_{S1}) will vary by less than 15 percent for a 4:1 variation of Z_{01} ; i.e., for $0.5 \leq (X_j/2 Z_{01}) \leq 2.0$. Thus, the loaded Q of the signal circuit is not a critical function of Z_{01} .

The expression for R'_g is given¹² to be

$$R'_g = \frac{R_s}{A} \left(\tilde{Q}_{es}^2 \frac{f_s}{f_1} - 1 \right) \quad (2-15)$$

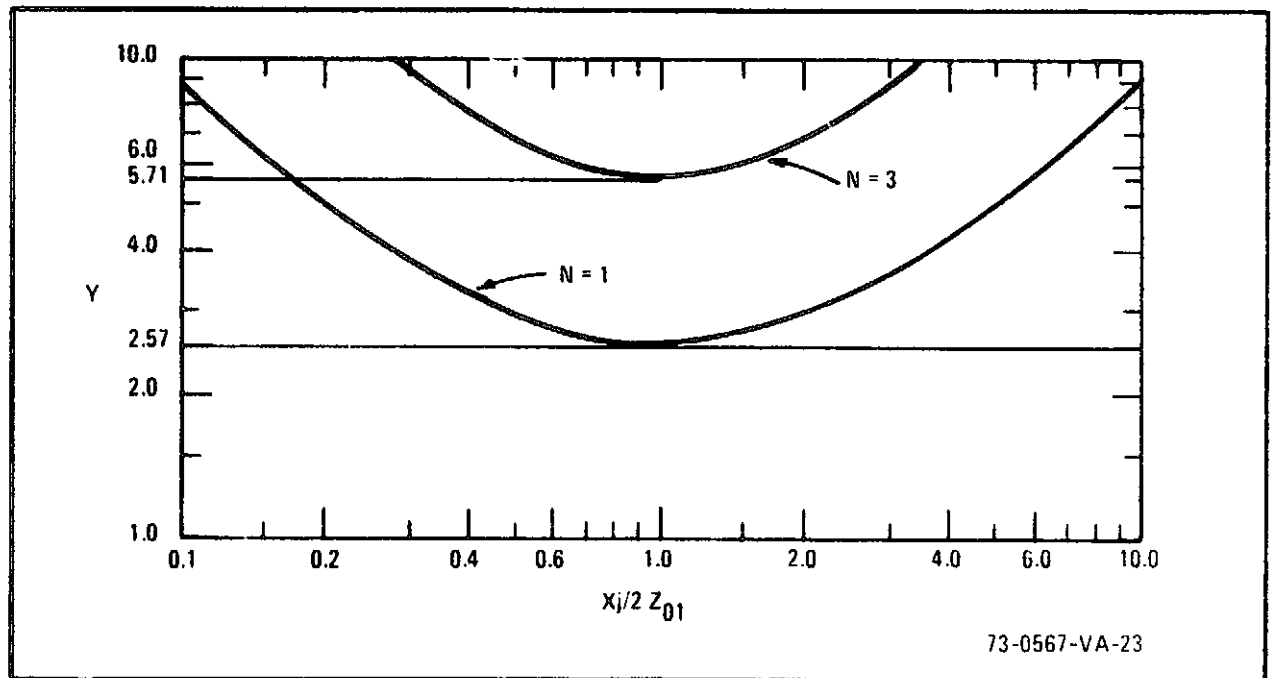


Figure 2-35. Signal Circuit Impedance Inverter Parameter, Y

where

$$A = \frac{\sqrt{G} - 1}{\sqrt{G} + 1} \quad (2-16)$$

and G is the actual negative resistance power gain at the varactors. In paragraph 2.2.2.1, the dynamic signal Q was shown to be $\tilde{Q}_{es} = 12$. Then, for a diode gain of 18 dB (for an overall paramp gain of 17 dB) and using equations 2-15 and 2-16, the signal loading impedance is obtained, $R'_g = 70$ ohms. In the initial design, $Z_{01} = 50$ ohms. The junction capacitance at the desired bias point has already been given as $C_j = 0.2$ PF (or $X_j = 66$ ohms). Thus, $X_{SH} = 76$ ohms, which leads to a value for the tuning capacitance, $C_T = 0.17$ pf. In paragraph 2.2.2.1, the signal circuit cutoff frequency degradation factor was taken to be $k = 2$. So that, by equation 2-12, the shunt loss term is found to be $R_{SH} = 3,268$ ohms. Now the circuit at point 2 will resemble

that of a simple parallel tuned RLC circuit with an unloaded $Q = R_{SH}/X_{SH} \cong 43$, and a loaded Q (from equation 2-14) of $Q_{S1} = 1.10$. The signal load impedance at point 2 required to give the prescribed value of r'_g is simply Z_{01}^2/R'_g . As the second resonator length is in multiples of half wavelengths, and the signal source impedance is R_g , then the impedance inverter (transformer) is characterized by having a length of one quarter wavelength and a characteristic impedance, Z_{02} , is given by

$$Z_{02} = \left(\frac{R_g}{R'_g} \right)^{1/2} Z_{01} \quad (2-17)$$

As $R_g = 50$ ohms, $R'_g = 70$ ohms, use of equation 2-17 yields $Z_{02} = 42$ ohms.

If the second resonator is not used (if substrate -2 is replaced with a simple straight through section of 50 ohm line) then a single tuned response will be had with a gain-bandwidth product prescribed¹⁴ by

$$\sqrt{G} b = \frac{2}{Q_{S1} + Q_i \frac{f_s}{f_i}} \quad (2-18)$$

where b is the fractional bandwidth (Bw/f_s) and Q_i is the idler Q and is given as

$$Q_i = \frac{f_{ci}}{f_i} \quad (2-19)$$

Using numbers already generated, it can be shown that a single tuned bandwidth of 180 MHz can be expected with a gain of 18 dB. The calculated value of $Q_i = 36.0$; the value of $Q_{S1} = 1.1$. Thus it is obvious that in this case the idler circuit has dominating influence of the paramp $\sqrt{G} b$.

Use can be made of equation 2-18 to determine Q_i quite accurately.

Once the single tuned design has been performed, and the parameters optimized

for maximum \sqrt{G} b, then it is a simple matter to measure $^{18} Q_{S1}$, and calculate from equation 2-18 the actual value of Q_1 .

Now the double tuning comes about as follows. The second resonator, being multiple half wavelengths long and of characteristic impedance $Z_{03} < R_g$, causes the source signal impedance at point 3 to resemble that of a simple parallel tuned RLC circuit. The adjacent quarter wave impedance transformer with characteristic impedance Z_{02} , provides an impedance inversion so that the signal source impedance at point 2 will resemble that of a simple series tuned RLC circuit which combines with the parallel resonance of the first resonator to produce the required double tuned response.

The loaded Q of the second resonator can be given in terms of the number of quarter wave sections (N) and the ratio of the characteristic impedance (Z_o) to the resonator load impedance, R_g . More specifically, any in-line resonator of length ($N\lambda/4$) will have an input immittance which will resemble that of a simple parallel or series tuned RLC circuit and will have a loaded Q given by the following

$$Q = \frac{N\pi}{4} \left(\frac{1 - y^2}{y} \right) \quad (2-20)$$

where

$$y = \frac{Z_o}{R} \quad \text{or} \quad \frac{R}{Z_o} \leq 1 \quad (2-21)$$

The following four cases apply.

- (1) Series Resonance: $Z_o < R$; $N = 1, 3, 5, \dots$
- (2) Series Resonance: $Z_o > R$; $N = 2, 4, 6, \dots$
- (3) Parallel Resonance: $Z_o < R$; $N = 2, 4, 6, \dots$
- (4) Parallel Resonance: $Z_o > R$; $N = 1, 3, 5, \dots$

The curve of Q versus the filter parameter y is given in Figure 2-36. For the present application, case (3) will apply.

It can be shown that the reflection coefficient, Γ , referred to point 4 in the signal circuit can be given by

$$\Gamma = \frac{f(g) + f(v)}{f(g) - f(v)} = |\Gamma| e^{j\theta} \quad (2-22)$$

where

$$f(v) = \frac{1 - Q Q_1 v^2 - j (Q_1 Q_2 Q v^3 + Qv - Q_2 v)}{1 + Q_1 Q_2 v^2 - j Q_1 v} \quad (2-23)$$

$$f(g) = \frac{\sqrt{G_o} - 1}{\sqrt{G_o} + 1} \quad (2-24)$$

and the following definitions hold.

$$v = \frac{2 \Delta f_s}{f(g)} \quad (2-25)$$

$$Q_1 = \frac{Q_{S1}}{f(g)} \quad (2-26)$$

$$Q_2 = Q_1 \frac{f_s}{f_i} \quad (2-27)$$

$$Q = Q_{S2} f(g) \quad (2-28)$$

Q_{S2} = loaded Q of the second signal resonator.

The power gain of the amplifier is given by

$$G(v) = |\Gamma|^2 \quad (2-29)$$

and

$$G(v) = G_o$$

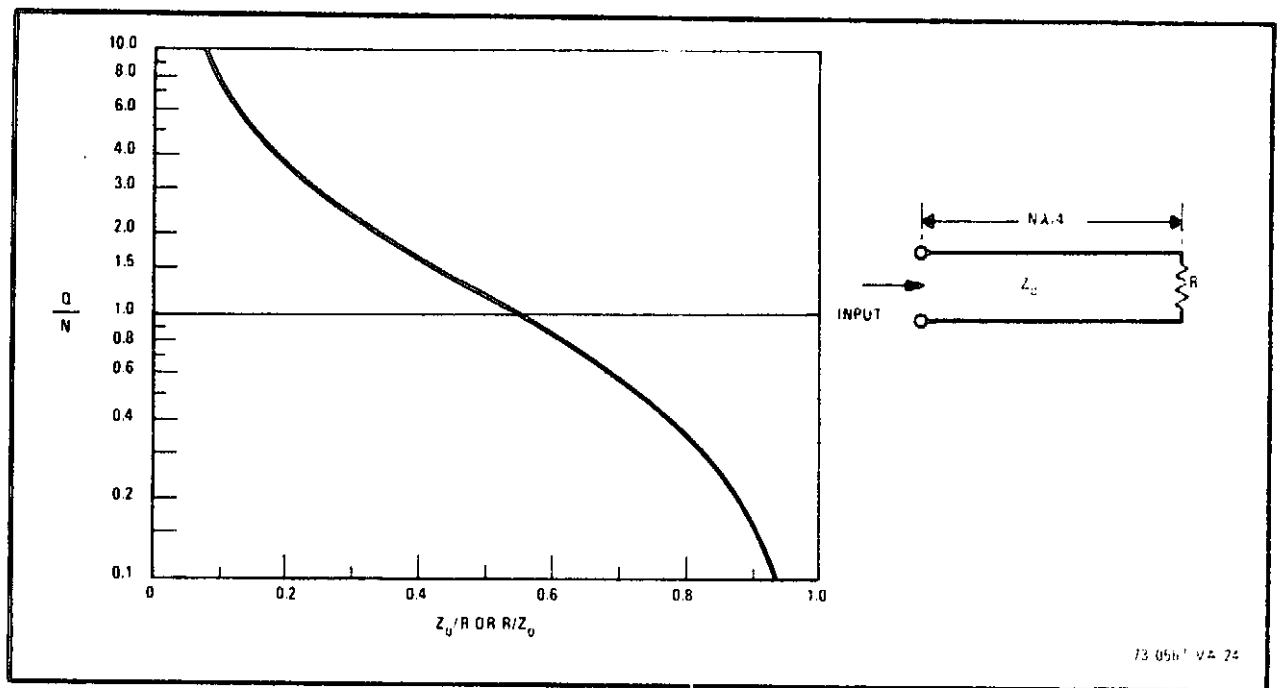


Figure 2-36. Loaded Q of In-Line Resonator of Length $N\lambda/4$

The above equations allow full characterization of the frequency response of the paramp, including gain, phase, phase linearity, etc.

Once the center band gain has been specified and Q_{S1} and Q_i determined, Q_{S2} can be determined from equation 2-22, and the specification of a given amplitude response slope. The condition for a maximally flat response imposes an additional constraint of Q_{S1} (relative to Q) which says that we are no longer able to rather arbitrarily specify Z_{01} , as was previously implied. Connors¹⁵ has shown that for the maximally flat condition, the signal and idler Q 's are related, and it can easily be shown that the relation can be put in the following form.

$$Q_{S2} = Q_i \frac{f_s}{f_i} \quad (2-30)$$

and

$$Q_{S1} = \frac{2 Q_i}{\sqrt{G_o} + 1} \frac{f_s}{f_i} \quad (2-31)$$

Now using the Q's obtained earlier ($Q_{S1} = 1.1$ and $Q_i = 36.0$), the amplitude response was obtained assuming no more than 0.1 dB slope to the gain frequency characteristic, and both a 14 dB and an 18 dB value for midband gain. Because of the losses in the circulators, this corresponds to an overall paramp gain of 13 dB and 17 dB.

Figure 2-37 presents the calculated single - tuned response ($Q_{S2} = 0$) for $Q_{S1} = 1.1$ and $Q_i = 36$ and 13 dB overall gain. Setting $Q_{S2} = 0$ implies that the length of the second resonator goes to zero. For the given set of values Q_{S1} , Q_i , a value for Q_{S2} is determined. This value of Q_{S2} is simply realized by setting the length of the second resonator to $N\lambda/2$ and selecting its proper characteristic impedance according to equation 2-20 or the data in Figure 2-36. The second curve in Figure 2-37 is the response curve for double tuning. The bandwidth improvement by double tuning the input is impressive and realizable. The 1 dB bandwidth for this condition is about 1.46 GHz, the 3 dB bandwidth is about 1.63 GHz, both well in excess of contract requirements.

Figure 2-38 shows the actual breadboard design goals. These results are similar to those of Figure 2-37, but with the circuit adjusted for an overall gain of 17 dB. The 1 dB bandwidth is seen to be 1.17 GHz (12.6%), still well in excess of the requirement. The bandpass ripple is only 0.3 dB max and is half that encountered in the lower gain, broader band design.

If one desired a maximally flat response, the conditions imposed by equations 2-30 and 2-31 must be observed. Note that both Q_{S1} and Q_{S2} are given in terms of Q_i . But Q_i is just (f_{ci}/f_i) , assuming no other idler circuit loading. Thus, selection of the idler frequency, and the diode with its f_{co}

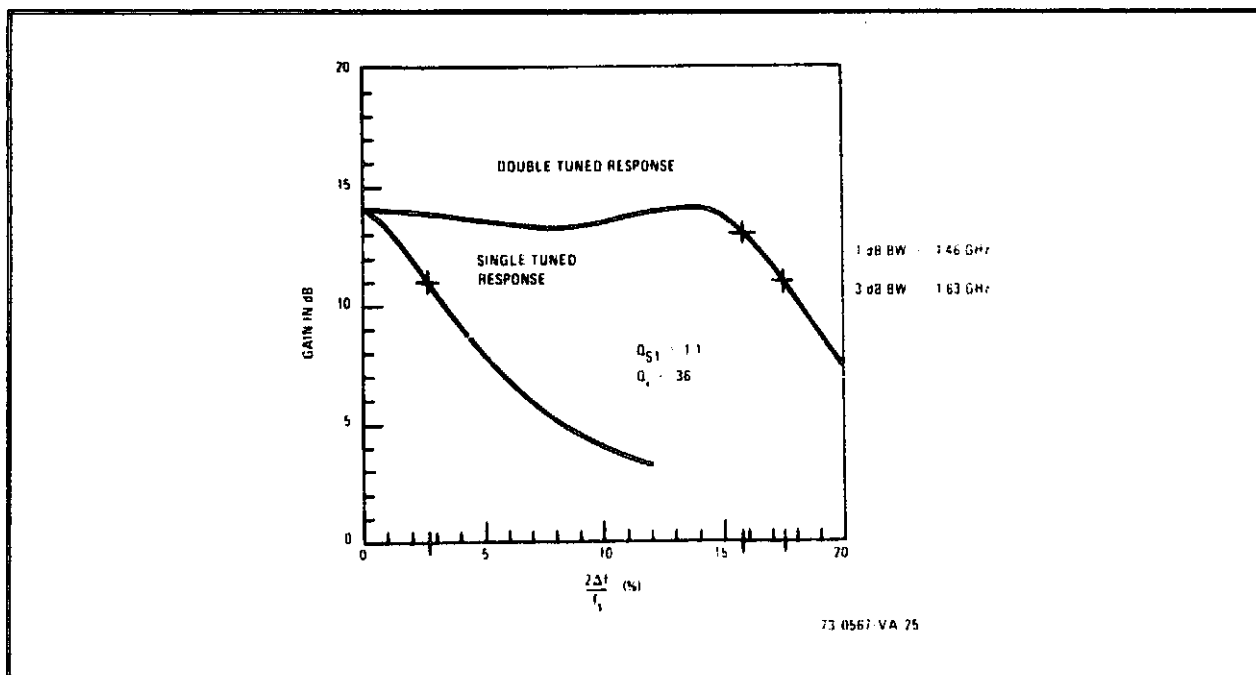


Figure 2-37. Gain vs Bandwidth -- Breadboard Design for Minimum Gain and Maximum Bandwidth

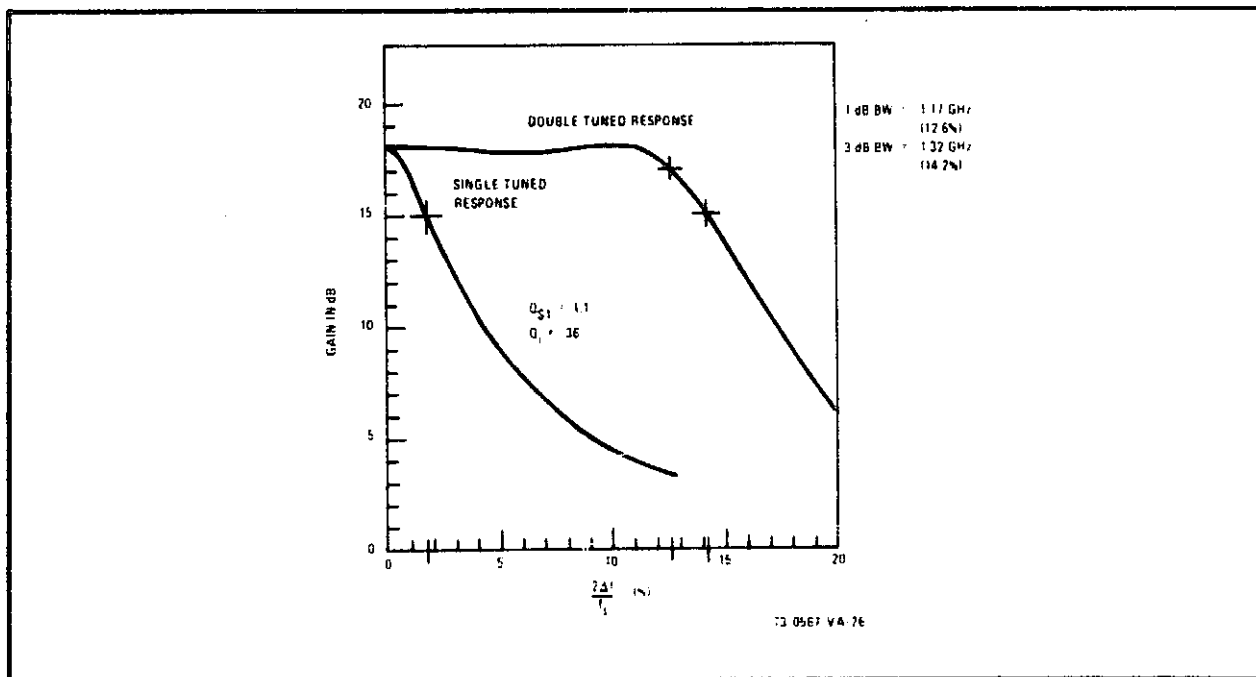


Figure 2-38. Gain vs Bandwidth -- Breadboard Design Goal

determines Q_i and thus the bandwidth. But the idler circuit can be loaded in two ways. Resistive loading will lower the Q and increase bandwidth; but this, concomitantly, will increase the noise figure and is thus undesirable. The idler can be reactively loaded which will not affect the noise figure but will only serve to increase the idler Q rather than decrease it. Then, examination of equations 2-30 and 2-31 shows that for a given Q_i and required gain, there is a specific value for both Q_{S1} and Q_{S2} . Both of these values are under the designers control simply through adjustment of the three signal line characteristic impedances, Z_{01} , Z_{02} , and Z_{03} . Essentially, Z_{01} effects Q_{S1} , Z_{02} sets the gain, and Z_{03} effects the required Q_{S2} . Figure 2-39 presents the calculated response of a design for a maximally flat bandpass. The idler Q is again taken to be 36, Q_{S1} and Q_{S2} are set by equations 2-30 and 2-31. The calculation was performed for both the 14 dB and 18 dB gain cases. The response is in fact very flat but an appreciable loss in bandwidth is encountered because of the required increases in Q_{S1} . Note that Q_{S2} has not appreciably change from prior calculations. The 1 dB bandwidth in this case is only 0.63 GHz (6.7%) with a 3 dB bandwidth of 0.78 GHz (0.4%). The only way to improve the maximally flat bandwidth would be to increase the idler frequency. Note however, that Q_{S1} and Q_{S2} vary inversely with the square of the idler frequency, so small changes in f_i can mean appreciable changes in bandwidth. Note also that as f_i increases, the noise figure is reduced, so it is wise to use as high an idler frequency as is possible. In the present case, as we are working with MIC techniques we are limited; and also because of the signal level (saturation assumptions) a relatively large junction capacitance is being used. This makes the task of resonating the idler very difficult.

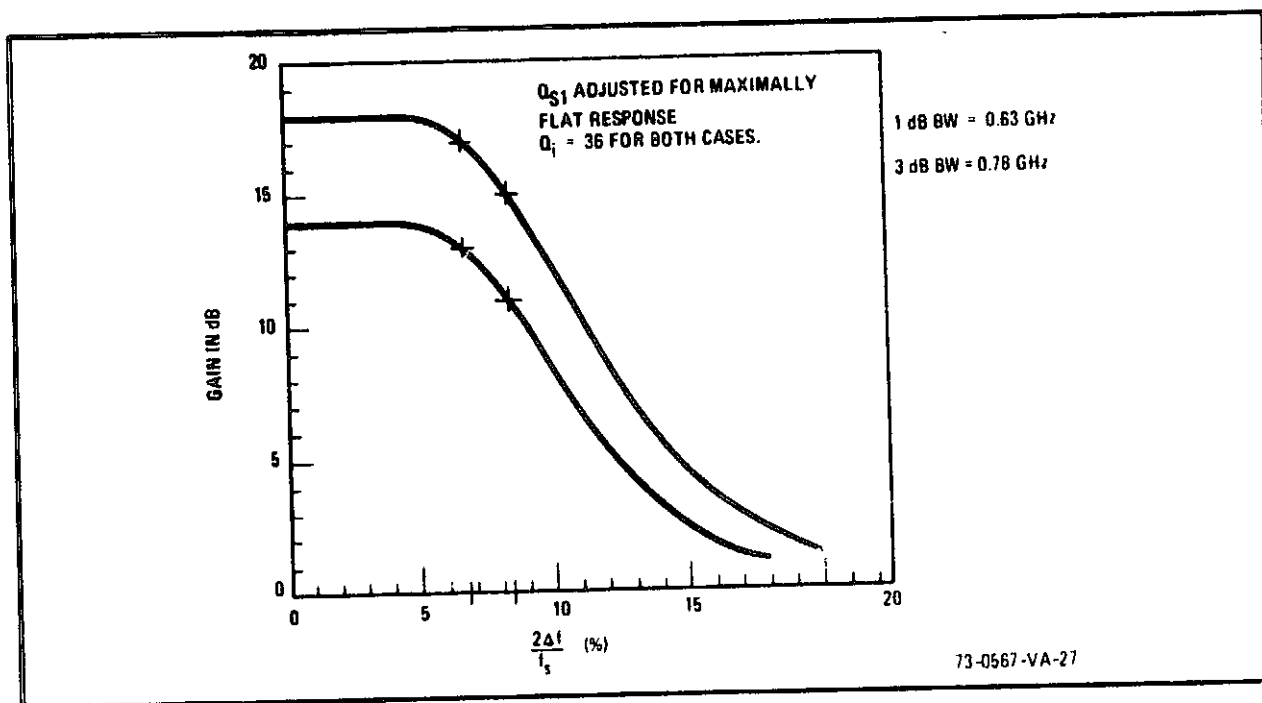


Figure 2-39. Gain vs Bandwidth of a Design for Maximally Flat Bandpass

Thus the idler frequency of 24 GHz is a compromise, but the results presented in Figure 2-38 make it appear to be an acceptable compromise.

2.2.2.5 Phase Linearity

The phase (θ) of the paramp signal circuit reflection coefficient primarily determines the linearity of the paramp. Figure 2-40 shows the calculated phase characteristics of each of the four designs presented in Figures 2-37, 2-38, and 2-39. To determine phase linearity, the phase response was first plotted, then a best fit straight line approximation was made. The difference between the true phase curve and the straight line approximation was taken to be the phase deviation from linear. For the 17 dB gain amplifier, the maximum deviation is about 3.5 degrees over the center 10 percent of the band. For the 13 dB case, it is on the order of a 1.0 degree over 10 percent band and 3.5 degrees to 12 percent.

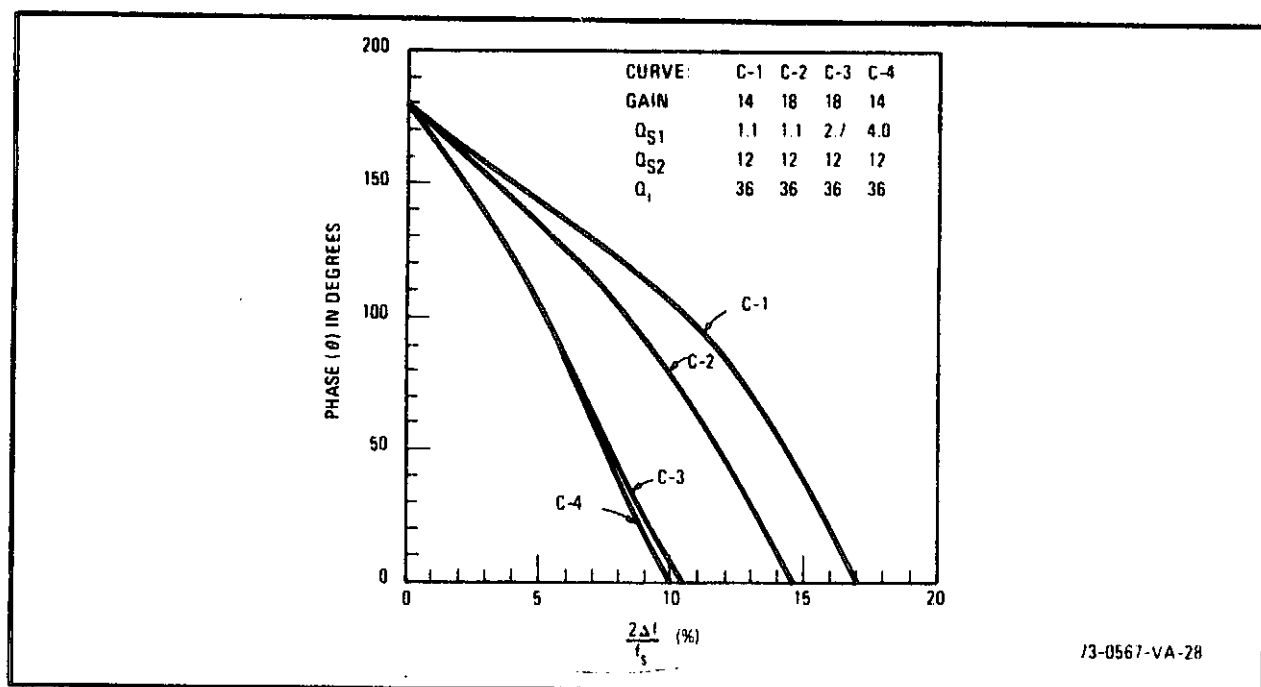


Figure 2-40. Phase, θ , vs Bandwidth

2.2.2.6 Gain and Phase Stability

To minimize the noise contributions from the subsequent circuits, the power gain of the paramp should be as high as possible. However, the maximum gain usable in practical designs is limited by the required gain and phase stability of the amplifier. The paramp is a negative resistance device, and both the gain and transmission characteristics are susceptible to pump power and circuit impedance variations. For a low noise, high gain amplifier with an 18 dB gain, the gain changes by about 0.1 dB for an 0.013 dB change in pump power. The change in gain for a given change in pump power is

$$\frac{\Delta G}{G} = \frac{G - 1}{\sqrt{G}} \frac{\Delta P}{P} \quad (2-32)$$

where

G = initial gain

P = initial pump power

ΔG = variation in gain

ΔP = variation in pump power

This expression is valid only for small changes in pump power, and gives the slope of the gain vs. pump power curve for a particular initial gain.

The phase stability relates directly to gain stability, as well as any circuit changes caused by environmental changes. The circuits changes due to temperature variation will be stabilized by the usual temperature stabilization or compensation techniques. However, a phase change due to a gain change caused by pump power change can be predicted¹⁴ and is well approximated for abrupt junction varactors by

$$\Delta\theta = .25 \tilde{Q}_{es} \frac{\Delta G}{G} \frac{f_s}{f_i} \left[\frac{\tilde{Q}_{es} - \left(\frac{f_i}{f_s}\right)^2}{\tilde{Q}_{es}^2 - \frac{f_i}{f_s}} \right] \quad (2-33)$$

Thus the change in phase (in degrees) for a given change in gain resulting from changes in pump power can be given for the breadboard paramp by the simple expressions

$$\Delta\theta = 71 \frac{\Delta G}{G} \text{ in degrees} \quad (2-34)$$

or

$$\Delta\theta = 553 \frac{\Delta P}{P} \text{ in degrees} \quad (2-35)$$

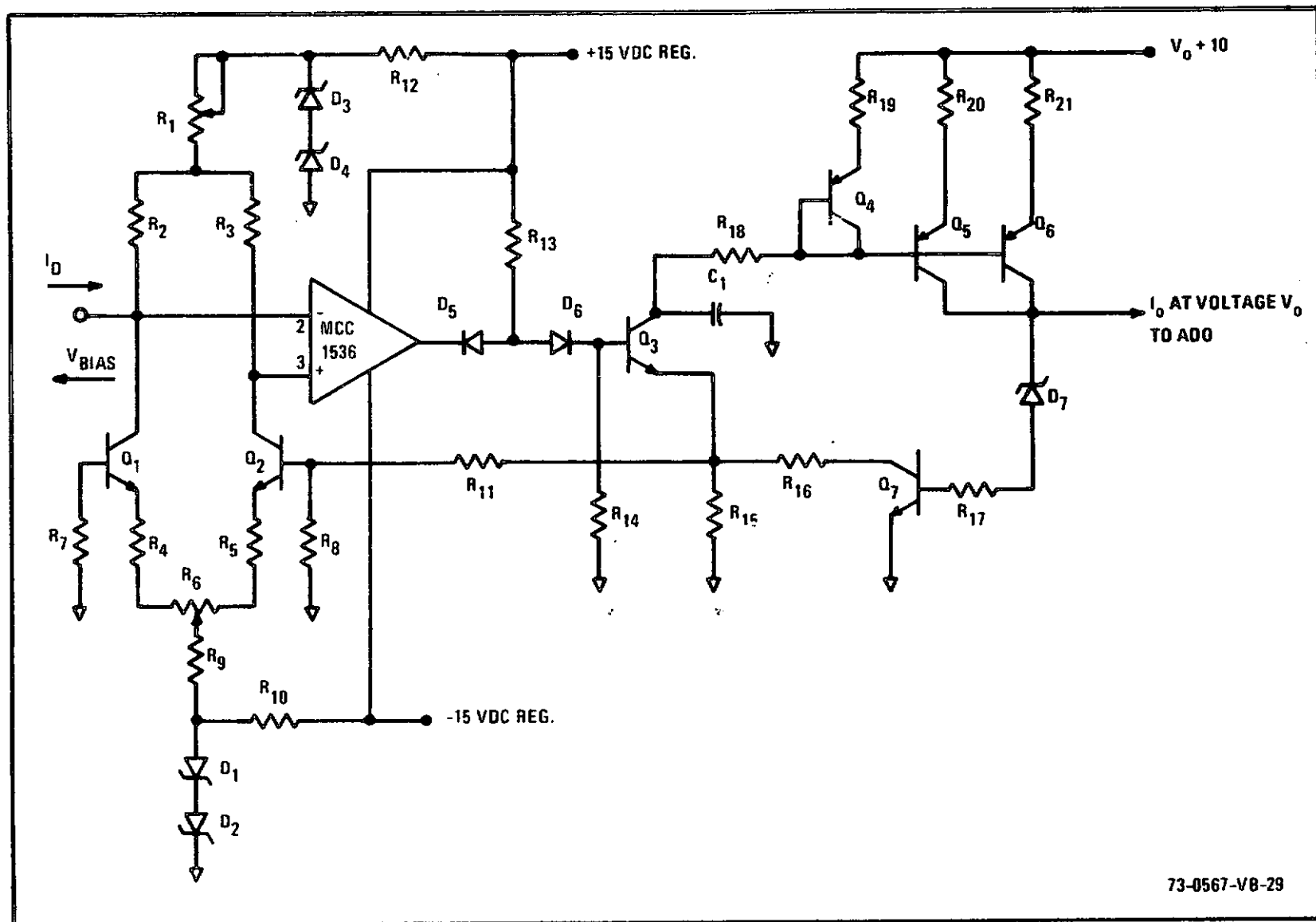
This translates to about 1.65 degrees phase change for 0.1 dB gain change, or about 13 degrees phase change for 0.1 dB change in pump power.

2.2.2.7 Varactor Bias Regulator and Pump Leveling Circuitry

Temperature variations will cause changes in signal and idler resonance primarily due to the temperature effect on the varactor diode junction capacitance. The junction capacitance per unit area is given as $[(q \epsilon N/2 (\phi - V))]^{1/2}$. As ϕ is a function of temperature, so is the junction capacitance. But this effect can be countered by simple compensation within the varactor bias regulator.

As the paramp gain and phase characteristics are both sensitive functions of pump power and varactor bias voltage, and as the paramp must operate unattended for so long, it is certain that the residual small circuit changes with temperature and time will conspire to give trouble if the actual pump power and bias voltage into the varactors are not regulated. Thus the paramp design contains an integral voltage regulator to ensure varactor bias stability (and compensation) and a varactor current sampling circuit and feedback amplifier which acts to control and regulate the RF pump power actually being supplied to the varactors.

Figure 2-41 is a circuit diagram of the regulator and control circuit (to be used with IMPATT pumps) which has been breadboarded and tested has been converted to integrated circuit form. The diodes D_1, D_2, D_3, D_4 are avalanche regulator diodes which have essentially zero temperature coefficient. Resistors R_1, R_2 , and R_3 are one-half of a bridge circuit which sets the varactor diode bias voltage (V_{bias}) and simultaneously samples the varactor current (I_D). R_1 is the bias adjustment control. Resistors R_4, R_5, R_6 , and R_9 in conjunction with the transistors Q_1 and Q_2 comprise a pair of balanced constant current sources which complete the lower half of the input bridge circuit.



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Figure 2-41. Varactor Bias Regulator and Pump Power Leveler Circuit

R_6 is the balance adjustment which sets the difference in collector currents between Q_1 and Q_2 . When pump power is applied to the varactors, the power is increased until the diodes rectify some of the RF power and supply current I_D to the bridge to offset the unbalance between collectors Q_1 and Q_2 . This is the regulating mechanism. The unbalance in the two currents is sampled by the Motorola high gain operational amplifier (Op Amp) which amplifies the unbalance (error signal) and applies this signal to the base of transistor Q_3 . Transistor Q_3 with the emitter resistor R_{16} comprise a voltage to current converter. The collector current of Q_3 is now proportional to the error voltage. It is amplified by the transistors Q_5 and Q_6 which now supply the required current I_0 to the Avalanche Diode Oscillator. The impedance of the current source I_0 is very high (essentially a constant current source) even at frequencies of tens of megahertz. This is a basic requirement for the stability¹⁹ of the Avalanche Diode Oscillator and its low noise operation.

A prime feature of the bridge input circuit is that the bias voltage and the diode current adjustments are independent of one another. During paramp operation and setup, the bias voltage can be adjusted while the regulator ensures a sufficient supply of pump power to maintain a given drive in the diode. Also the pump drive can be adjusted and regulated to any value from a few nanoamps to tens of microamps.

The current output drive stage is protected against IMPATT failure by short circuiting. The IMPATT normally will be operating at some voltage, V_0 . The voltage drop across the transistors Q_5 and Q_6 and the resistors R_{20} and R_{21} is about 10 volts. If the output is shorted, the increased power dissipation in the transistor would cause permanent damage if the output current were not immediately reduced. The diode D_7 is an avalanche regulator diode whose

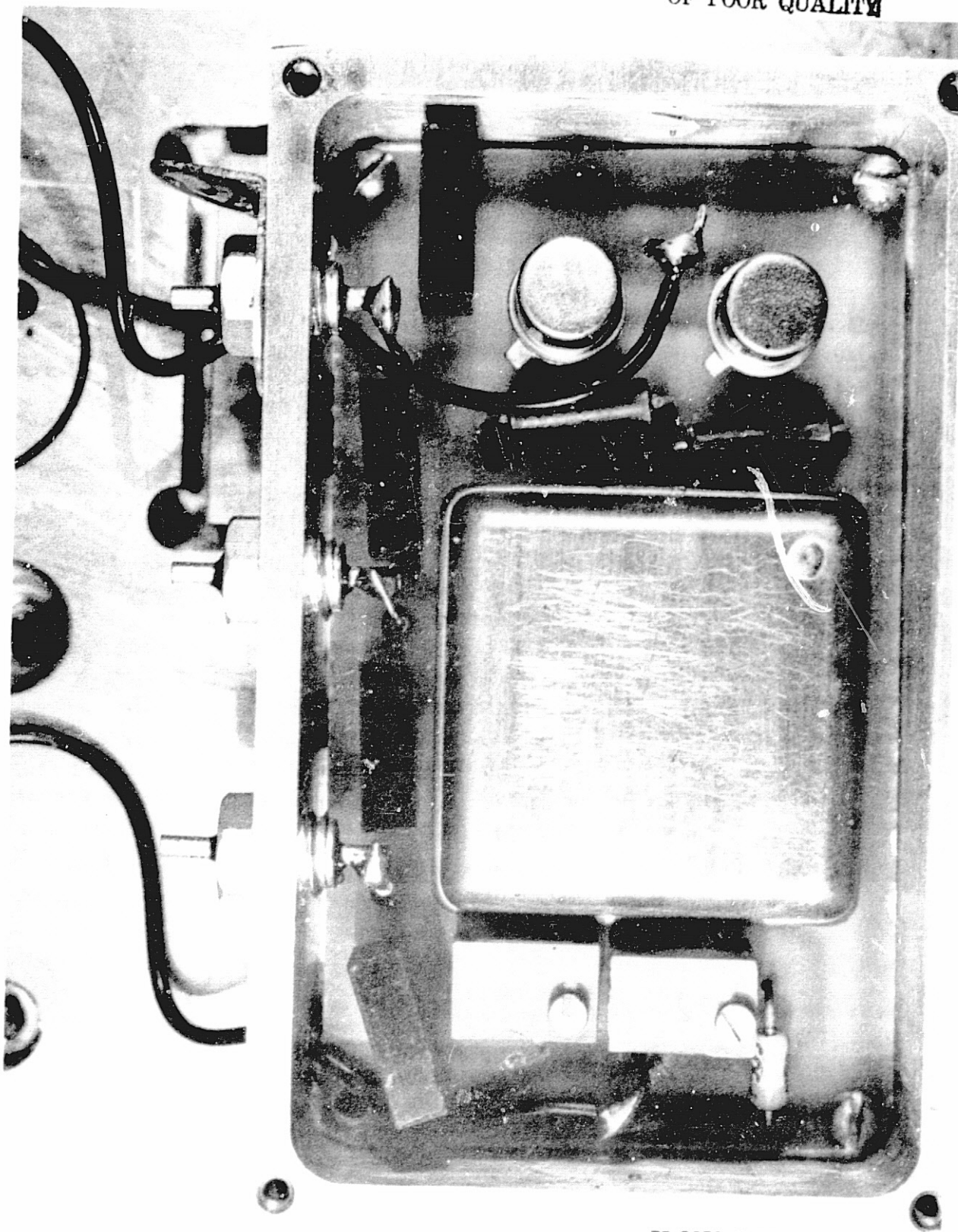
voltage breakdown is about 10 volts less than V_0 . As long as the output voltage is greater than the breakdown of D_7 then current passes through the base of transistor Q_7 which is held in saturation, and R_{16} (150 ohms) will determine the output current for a given voltage at the base of Q_3 . If the output is shorted, D_7 and also Q_7 turn off. This removes R_{16} from the current path and R_{15} (6.2 Kohms) now sets the output current at only 2.5 percent of the initial value and well inside the damage level for Q_5 and Q_6 .

The test results on the breadboard version showed the design to be fully satisfactory. A load simulator, comprising a pair of Zener regulator diodes, current sensing resistors, and a feedback terminal, was assembled and used to test the overall ability of the regulator and leveler circuit to maintain a constant current, I_d , over a broad temperature range and large variation in output power. The load simulator was maintained at constant temperature while the breadboard regulator was operated over the temperature range of -50°C to $+100^\circ\text{C}$. With fixed load, and the diode current $I_D = 1.0$ microampere, a variation of only 14 nanoamperes is encountered in operation across the full temperature range. This corresponds to a variation of only 0.012 dB of the RF power into the varactors. For a 6 dB change in the output power attenuator, the regulator power was held sufficiently constant so as to allow only about 2.0 nanoampere change in I_D , which corresponds to a variation of only 0.002 dB of rf power change into the varactors.

The circuit diagram for the breadboard version of the bias regulator and pump leveler was given in Figure 2-41. The circuit was then reduced to hybrid microelectronic form with the majority of the components being used in chip form and being mounted in a microelectronic circuit package. The breadboard, which measured 2.5 x 5.0 inches, has been reduced in size and placed

inside a microelectronic package which measures about 0.8" x 0.8". Adding dc input terminals and line filters and mounting the microelectronic package on a printed circuit board with the two final driver transistors and the bias voltage and pump level control potentiometers, yields an overall board size of nominally 1.0 x 2.0 inches. A photograph of the complete circuit is shown in Figure 2-42.

The performance is essentially as measured for the breadboard version. Final performance tests were to be performed with an operating paramp. Means are available in the regulator circuit for temperature compensating the performance. These means have been adjusted by considering only the stability of the bias voltage and rectified diode current. However, final adjustment would be made by considering the paramp stability and obtaining best paramp performance over temperature.



73-0939-P-14

Figure 2-42. Varactor Bias Regulator and Pump Leveler Circuit

3. SUMMARY AND CONCLUSIONS

During the period of this program, the effort has been concentrated in two specific areas; namely, the development of a low cost paramp and the development of a low cost low noise down converter.

Although the stated paramp objectives of low cost and high performance were not attained, excellent results were obtained in the development of the down converter. New and unique techniques for image enhancement have been devised which have led to a mixer with a conversion loss of under 4.0 dB for an instantaneous bandwidth of .35 GHz in converting from 12 GHz to 2.6 GHz 1F. The best results with the paramp included a noise figure of 2.5 dB with a gain of 15 dB and a bandwidth of 120 MHz. These paramp results, however, could not be reproduced; and once attained, could not be readily stabilized with time and temperature.

Several severe problems of a fundamental nature were encountered. The first, and most severe, relates to the use of slot-line for pump transmission to the varactor diodes. The problem rests on the inability to control and resonate the idler in the immediate vicinity of the diodes. A second problem exists because of the radiative nature of the slot-line. A third problem relates to the difficulty in obtaining a simple, well controlled idler resonance around the varactors and stems from the intended use of conventional wire bonding (ball bonding and wedge bonding) techniques for contacting the diodes.

A result of the above noted problems is the recognition of severe limitations to the feasibility of using the slot-line coplanar line configuration

for MIC paramps. The initial approach is now considered to have been overly ambitious and a fallback position is now being recommended.

The functions which can be readily integrated are the ferrite circulator and the bias insertion filters. These two functions can be combined in an electrically efficient and cost effective manner. Thus, it is to be recommended. However, the integration of the signal and idler circuits with chip diodes is not recommended because of the lack of test point interfaces. That is, there are insufficient means of testing the individual parts to ensure that, upon assembly, the whole will perform as expected. It is recommended that packaged varactors be used which incorporate the package resonance as the idler resonance. Then this packaged varactor be embedded in a simple waveguide and coaxial circuit.

The key to low cost will be the use of a minimum number of machined parts combined with a mechanical assembly design which lends itself readily to ease of testing separate (signal, idler, pump) circuit resonances, as well as the use of the combined 5 - port junction circulator and the bias insertion and signal isolation filters.

It is believed that exploitation of the recommendations of this fallback position will lead to the attainment of a reliable, reproducible paramp satisfying reasonable system requirements (electrical and environmental) while meeting a cost goal of less than \$2,000 per paramp in quantities on the order of 200 units.

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